SINGLE EVENT UPSET TEST AT THE CRYRING HEAVY-ION ACCELERATOR *

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The energy and particle intensity domain of the CRYRING heavy-ion accelerator is well suited for studies of Single Event Upset phenomena. This effect occurs when a charged particle hits a working electronic circuit and the charge created alters its state. The radiative environment is one of the major problems for electronic circuits in an orbiting satellite. The situation is similar for future detectors at the new high-energy physics facilities, like the Large Hadron Collider (LHC) at CERN. The increasing use of submicron technology in combination with a lowering of the circuit voltage decreases the critical charge for temporary upsets. In this article the SEU test setup at CRYRING is described, where memories are used for testing digital circuit technologies. For these tests two types of particle extraction is used and two types of scintillator beam monitors (BaF_2 and YAP) are described. Temporary, soft errors were recorded in static RAM memory circuits.

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1. Introduction

The radiative environment is one of the major problems for electronic circuits in an orbiting satellite. The relatively large number of charged particles, not only electrons and protons but also heavy ions either present in

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space or originating from the construction material, will affect semiconductor devices. The situation is similar for the future detectors of the new high-energy physics facilities, like the Large Hadron Collider (LHC) at CERN [1,2]. Here, the extremely large number of light particles, *i.e.* protons and pions might initialize nuclear reactions and recoiling nuclei cause damage to the crystal structure. The radiation environment thus will resemble to some extent that of the space. Also at ground level the energetic light particles might cause unwanted effects on electronic devices.

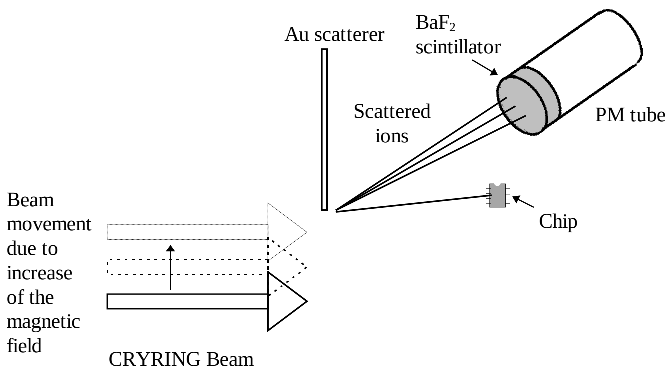

Fig. 1. The current measuring setup

2. Radiation

2.1. Radiation environments

At altitudes where satellites orbit cosmic rays are of major concern. The extremely energetic heavy ions, originating from the interstellar space have energies up to 10^{20}eV and atomic number up to $Z = 26$ (iron). These energetic cosmic rays can cause some problems even at ground level. Another source of radiation for orbiting satellites is particles in the Van Allen belt, which contain geomagnetically trapped electrons and protons and some heavier ions [3,4].

Similar problems with radiative environment will arise in the future high-energy physics detectors with front-end electronics close to the radiation source. The energetic light particles originating from collisions in the detectors create heavy recoiling ions which will irradiate the electronic circuits [1,2].

2.2. Electronics and radiation

It is possible to classify the errors created by radiation in different ways [4]. The radiation can cause temporary errors, i.e. the correct device function can be restored by rewriting the data or repowering the circuit. Permanent errors disable the whole device or a part of it forever. In some cases however annealing might help to eliminate permanent errors, but its usage is unlikely on satellites. However certain self-annealing will always occur because of the heat produced during normal operation.

The total accumulated radiation damage gradually degrades the performance of the device. For example a parasitic transistor can be opened in the device, which results in complete stop of a function and increased power consumption (latch-up). Powering down and up the circuit can eliminate this, but the increased power consumption can lead to a total device burnout. It is also possible to make a current sensing device which in advance powers down the circuit avoiding the burnout.

Single energetic ionizing particles can also cause errors, called Single Event Effects (SEE). The increasing use of submicron technology in combination with lowering of the circuit voltage decreases the critical charge for such temporary upsets. The most common error of this type is the Single Event Upset (SEU). In this case the charge created by a particle passing through a transistor in the device might be enough to change the state of the node, causing a temporary upset. After correcting the data there remains no effect of the upset. Another type of error caused by a single ionizing particle is Single Event Latch-up (SEL), which is a local latch-up. SEL is more difficult to detect than latch-up of a whole circuit since the current consumption increases only slightly. SEL can lead to local burnout or can even escalate to a full latch-up.

2.3. Avoiding radiation damage

To avoid radiation damage shielding is a possible solution in some situations. However on satellites the weight and space is restricted and therefore it is impossible to shield the electronics against the energetic heavy ions of cosmic origin [4]. Similarly in high-energy physics detectors the available space is limited and shielding is often not possible because of the location of the electronics. Furthermore, particles can not be stopped by the shielding, because it would reduce the sensitivity of the detectors placed outwards from the electronics.

In radiation hardened circuits special technologies have been developed to avoid the consequences of harmful radiation. Device layout modifications are made to increase the critical charge and different monitoring circuits are added to avoid fatal errors.

The major drawback of using rad-hard devices is their price, because of these modifications of technology and the low volume production the cost can be ten or hundred times higher than for standard devices [6]. In many applications, like commercial telecommunication satellites this is unaffordable and also lower level of radiation hardness is acceptable. In such a case radiation tolerant devices can be used. These are manufactured with standard technologies but with similar layout modifications and additional monitoring circuits as the rad-hard devices.

3. Rad-hard tests

3.1. Test sources

For checking the Integrated Circuit (IC) manufacturing processes for radiation hardness, test setups are needed where the different radiation environments can be simulated [4].

The gamma irradiation can be produced with different gamma sources. To simulate extremely energetic cosmic rays particle accelerators are used. Fission fragments from Californium-252 sources can be used for low-energy heavy ion irradiation. Laser beams can be used to transfer large amounts of energy to the device.

3.2. Test devices

Memory circuits, a major part of all electronic devices, are high-density components and have a large number of identical cells. All these properties qualify them as good test device for radiation hardness tests.

Today CMOS is the most frequently used technology for standard electronic circuits. The radiation tolerant devices are also manufactured with CMOS technology where the active part of the device is built up on an isolating wafer such as silicon-on-sapphire (SOS) or silicon-on-isolator (SOI).

4. Rad-hard tests at CRYRING

4.1. The test setup

The energy and particle intensity of the CRYRING heavy-ion accelerator is well suited for studies of Single Event Upset (SEU) phenomena [7,4].

During the SRAM irradiation the memory is powered and loaded with different bit patterns. After some time the data in the RAM is read back, and compared with the original set of values. If the irradiation has changed the data, the memory location and the bit patterns are saved for further analysis.

For the RAM irradiation tests a PC based test setup with operating software was developed. The software emulates the necessary signals for the RAMs to be tested, generates the test patterns, checks the read values and saves the registered errors.

A special chip manipulator was built for the tests and is placed in one of the straight sections of CRYRING. It is possible to move the chip relative to the beam and it is also possible to rotate it in order to vary the angle of incidence of the particles.

The CRYRING storage ring is not equipped with beam extraction facilities and the ions used for irradiation purposes have to be deviated from the beam orbit. Furthermore the multiturn acceleration requires Extreme High Vacuum (XHV). This is achieved by baking all parts of the ring to 250–300° C prior to the experiment. Therefore materials and components which are introduced into the vacuum must tolerate that temperature. For instance a special socket had to be constructed to hold the chip under test since no standard material can be used. The socket is made of MACOR ceramic with wire wrapped connections. The ceramic packaged chip is open for the heavy ions.

4.2. Extraction and monitoring

As mentioned above the necessary prerequisite for this type of tests is that ions are extracted from the accelerator and guided to the irradiation position.

In the experiments performed so far the accelerated ions are deviated from the normal beam orbit to hit a gold foil perpendicular to the beam by increasing the field of the dipole magnets [8]. The ions hitting the foil will scatter and create a shower of particles on the memory chip and on the monitoring window. A fixed angular relation between the chip to be tested and the BaF_2 scintillator monitor allows normalizing the test [9].

In the near future a much more efficient extraction will be used. The charge exchanged ions of the electron cooler, *i.e.* ions with charge one unit less than the nominal beam, will hit the device to be tested and by adjusting the electron cooler voltage the time of extraction can be regulated. In this way a considerable number of particles will be guided to the measuring position contrary to the existing scattering extraction where a large fraction of the ions are lost. The charge exchange method will be used for low intensity "exclusive" ions.

The monitoring is made with a YAP crystal which is also an inorganic scintillator, radiation resistant, robust and has relatively high light output. It is placed on a probe and can be manipulated and the scintillation light is projected to a PM tube outside the ring vacuum by a mirror and lens system [10].

5. Results

As mentioned above the temporary or permanent errors of the SRAM circuit are registered on-line during irradiation. A typical error pattern is shown in Fig. 2 for an SRAM circuit when bombarded with ^{40}Ar ions of energy 2.5 MeV/A.

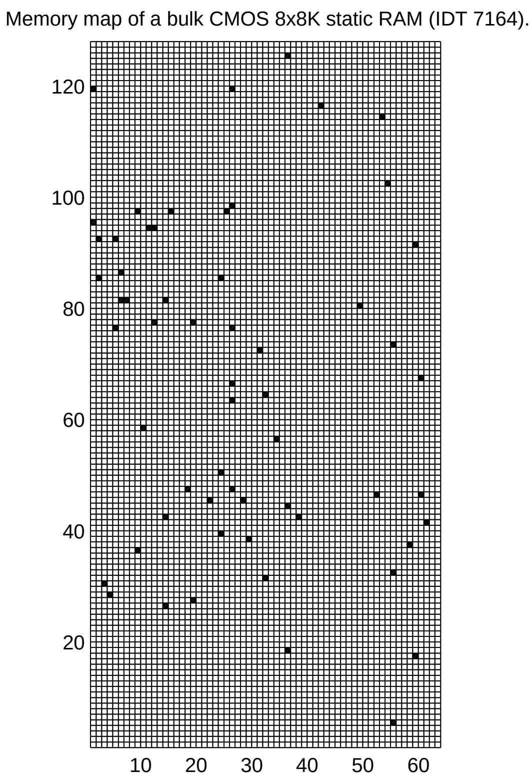

Fig. 2. Virtual memory map. The black areas are the memory cells, where temporary errors of Single Event Upset type were detected during irradiation.

The influence of particle type and energy and the angle of incidence of particles are the parameters to be investigated for different SRAM memory technologies. In Fig. 3 the angular dependence of the error rate is displayed for a standard CMOS circuit. A memory cell is assembled by several transistors, usually six, having asymmetric status for memory content 0 and 1. This asymmetry is reflected by the different error rates for logical 0 expected 1 observed or 1 expected and 0 observed. In Fig. 4 this asymmetry is displayed for the errors caused by 290 keV/A ^{40}Ar high intensity irradiation of the circuit.

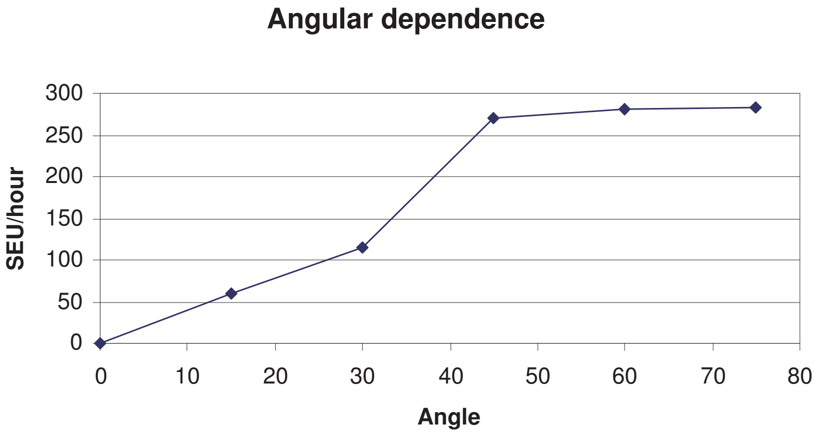

Fig. 3. Number of SEUs as a function of the beam incident angle to the chip

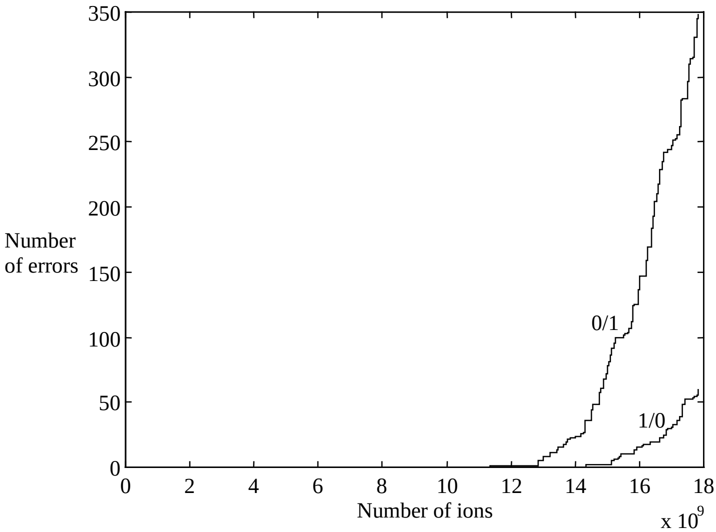

Fig. 4. Number of errors as a function of incident particles

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