EMULATION AND CALIBRATION OF THE SALT READ-OUT CHIP FOR THE UPSTREAM TRACKER FOR MODERNISED LHCb DETECTOR*

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The LHCb is one of the four major experiments currently operating at CERN. The main reason for constructing the LHCb forward spectrometer was a precise measurement of the CP violation in heavy quarks section as well as search for a New Physics. To obtain interesting results, the LHCb is mainly focused on study of B meson decays. Unfortunately, due to the present data acquisition architecture, the LHCb experiment is statistically limited for collecting such events. This fact led the LHCb Collaboration to decide to perform far-reaching upgrade. Key part of this upgrade will be replacement of the TT detector. To perform this action, it was requited to design new tracking detector with entirely new front-end electronics. This detector will be called the Upstream Tracker (UT) and the read-out chip — SALT. This note presents an overall discussion on SALT chip. In particular, the emulation process of the SALT data preformed via the software written by the author.

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1. Introduction

The Large Hadron Collider beauty (LHCb) detector is a forward single-arm spectrometer designed to cover acceptance in a range of pseudorapidity $2 < \eta < 5$. That geometry was optimized to collect as much B meson decays as possible. The study of such events could be essential to probe Physics Beyond the Standard Model or CP violation, and to characterise the nature of the underlying physics. Nevertheless, many of the interesting decay channels are statistically limited. However, the LHCb detector is not

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able to operate at current, delivered by the LHC accelerator, luminosity. The LHCb Collaboration decided to preform the upgrade. The main aim of the upgrade is to allow the spectrometer exploit the delivered luminosity up to 2×10^{33} [$\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$]. That expectation translates into amount of collected data equal to 50 fb^{-1} [1].

To obtain mentioned above goals, the new implementation of the front-end electronics must read out data at the bunch-crossing rate of 40 MHz. Therefore, it was decided that the new, designed in Kraków chip, will be able to digitalize analogue signal and subsequently make digital processing and zero suppression.

The emulation of the SALT's algorithms will be the key part of the maintenance of the future UT detector. In this respect, the quality of the designed software is crucial.

The remainder of the note is divided into three sections. The first one presents introduction to the problem being under consideration. Second section briefly describes the SALT read-out chip. The third one shows description and the performance study of implemented digital signal processing algorithms, which emulate SALT's ones. This section also presents all currently available calibrations procedures. The last paragraph summarizes the obtained results.

2. SALT read-out chip

SALT (Silicon ASIC for LHCb Tracking) is a read-out chip designed to replace the one currently widely used in the LHCb tracking system — Beetle. The novel of this chip comparing to the previous one is performance of digital signal processing and zero suppression.

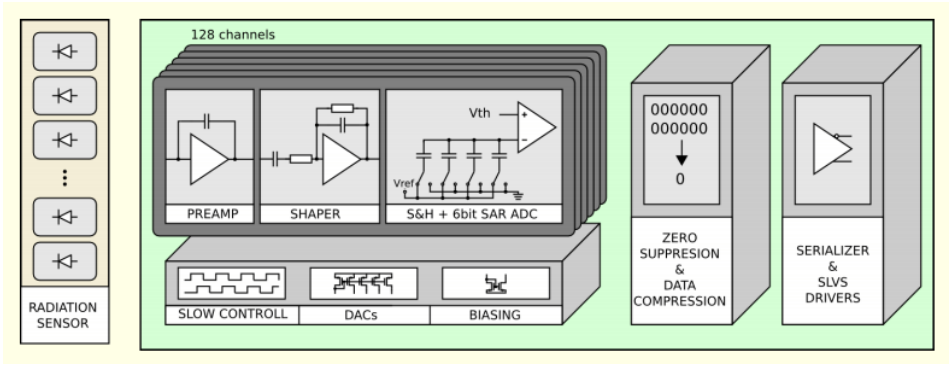

Fig. 1. Schematic view of the SALT chip [2].

The chip is made in IBM 130 nm technology. According to the design requirements, the SALT chip is able to read out data from 128 channels simultaneously. The second important SALT responsibility is to perform single channels analogue processing. To perform this process, the analogue pre-amplifier and shaper are implemented. After this preliminary processing, the signal is digitalized via the 6-bit successive approximation ADC. The next step, described more widely in the next session, is mentioned before digital processing and zero suppression. The schematic view of the SALT chip is presented in Fig. 1.

3. Emulation of the SALT algorithms

The crucial test of designed chip will be the comparison of the digital data with the ones emulated by the author's software, although this software will be also used in maintenance of the detection system. What is more significant, the presented software will be essential during the tuning of the chip's parameters. Accordingly, the software implementation of the emulated algorithms has to be as similar as possible to the SALT's HDL (Hardware Description Language) ones.

The SALT's digital processing is split into a few steps. First one is subtraction of the pedestal. In the next step, the common mode is subtracted. After that, the last step is a procedure called zero suppression.

This section describes each of these algorithms and monitoring plots.

3.1. Pedestal subtraction

The pedestal subtraction algorithm has two phases. In first, optional one, the pedestal values are calculated. This phase is also called training. During the second one, the determined pedestal values are subtracted from the raw ADC data.

3.1.1. Pedestal following

From the mathematical point of view, the calculation of the pedestal can be described as a running average. In every training event, the pedestal sum is updated. This update takes into account the previous value of the pedestal sum and the current ADC count. The pedestal sum is calculated for each channel separately. To be more precise, the pedestal sum, $p_i(n)$, for channel i and event i can be expressed as follows:

$$P_i^{\mathrm{sum}}(n+1) = P_i^{\mathrm{sum}}(n) + \frac{\Delta_i(n+1)}{N}\,, \tag{1}$$

where the $\Delta_i(n+1)$ is an event to pedestal correction. This correction is expressed as:

$$\Delta_i(n+1) = \mathrm{ADC}_i(n+1) - P_i^{\mathrm{sum}}(n)\,. \tag{2}$$

In equation (1), the N is the weighting factor set by default to 1024.

To increase the suitability of the pedestal, the limit for correction is applied. If the condition

$$|\Delta_i(n+1)| \leq 15 \tag{3}$$

is not fulfilled, the correction value is set to 15. To determinate the pedestal values, the pedestal sum should be normalized, so

$$p_i = \frac{P_i^{\mathrm{sum}}}{N}\,. \tag{4}$$

The initial value of the pedestal sums is set by default to

$$P_i^{\mathrm{sum}} = 512\ N[\mathrm{ADC}]\,.$$

3.1.2. Pedestal removing algorithm

The second phase of the pedestal subtraction algorithm is subtraction of determined pedestal values from the raw data. This procedure can be expressed as follows:

$$\mathrm{ADC}_i = \mathrm{ADC}_i^{\mathrm{RAW}} - p_i\,, \tag{5}$$

where ADC_i is signal value after pedestal subtraction for event i, $\mathrm{ADC}_i^{\mathrm{RAW}}$ is a raw data and the p_i is the pedestal value. Each of this quantities are in the unit of ADC counts.

3.1.3. Performance of the pedestal subtraction algorithm

The SALT chip is not ready yet, this fact led the author to use the Beetle's data to study the performance of the designed algorithms.

Figure 2 shows the exemplary monitoring plots of the pedestal subtraction algorithm. The right plot presents pedestal subtracted ADC values, all of them are well centred around the zero value. The pedestal values were obtained using 4096 training events, presented in Fig. 3.

It is worth noting that the SALT emulator allows to mask channels. This procedure is applied when one or more channels are broken. In that case, the signal in that particular channel is set to 0.

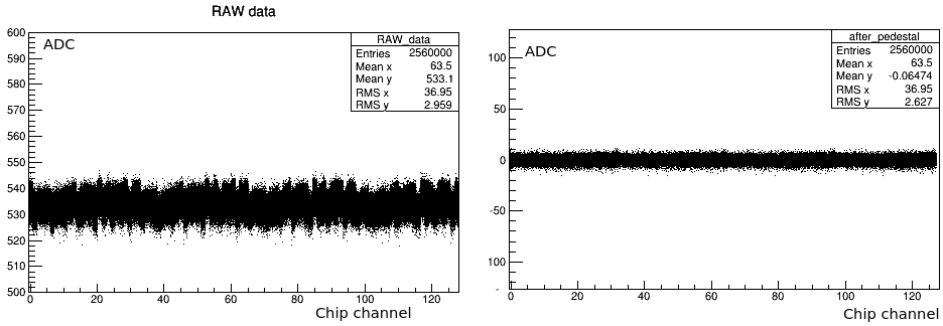

Fig. 2. Exemplary pedestal subtraction algorithm's monitoring plots. Typical raw (non-zero suppressed) data ADC values (left), pedestal subtracted ADC values (right).

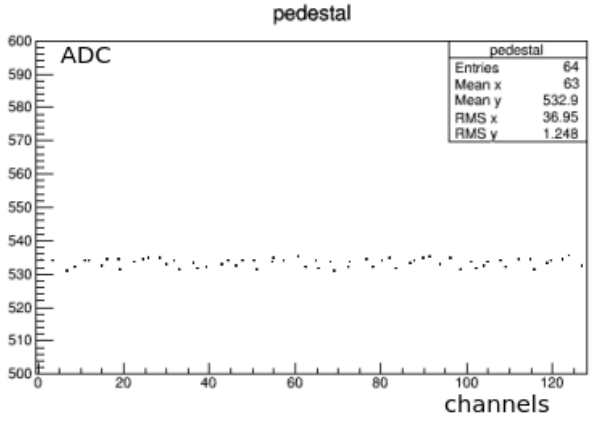

Fig. 3. Example of pedestal values.

3.2. Common mode subtraction algorithm

Currently implemented model of correction subtracts the mean common mode. The algorithm takes as an input data after pedestal subtraction. At the first stage, the common mode subtraction algorithm calculate the mean value of all channels, except channels with signal count bigger than parameter called hit rejection. The value of this parameter has to be tuned manually. Such a determined mean value, one correction number per event, is subtracted from each channels. Figure 4 presents the data after common mode subtraction.

This algorithm produces also a set of cluster thresholds, one number per channel. Cluster thresholds are understood to be noise values measured in each channel. The noise is mean to be RMS (Root Mean Square).

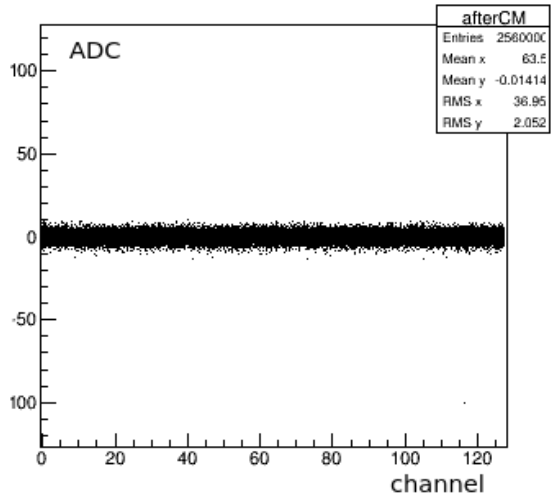

Fig. 4. Mean common mode subtracted ADC values.

3.3. Zero suppression algorithm

The last DSP (Digital Signal Processing) algorithm in SALT's processing chain is zero suppression. In this step, clusters are formed from the previously proceeded data. Predefined cluster thresholds, determined for each channel during common mode suppression process, are used in the cluster finding algorithm. In other words, this algorithm separates hits, also called signals, from the noise. Figure 5 shows noise data proceeded by the zero suppression algorithm.

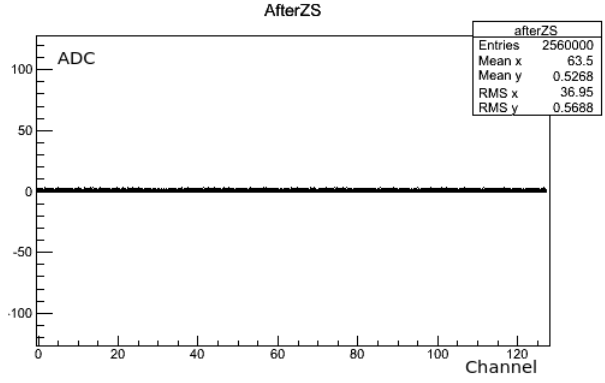

Fig. 5. Noise after processed by the zero suppression algorithm.

3.4. Calibration of the SALT's algorithms

One of the most important features implemented in the presented software platform is possibility of tuning run parameters. For instance, the calibration of pedestal subtraction algorithm's training entry can be preformed. In Fig. 6, the calibration plots are presented. According to this plot, it has been decided to choose 4096 as a sufficient number of training entry.

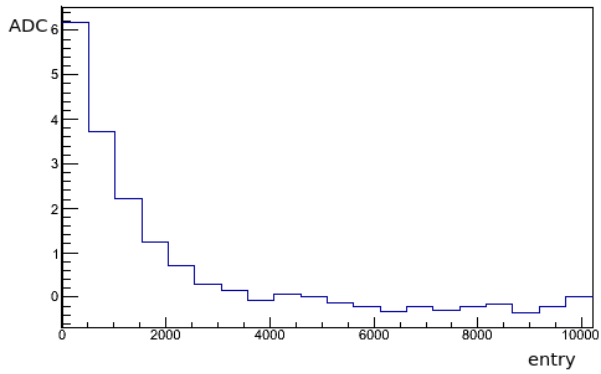

Fig. 6. Monitoring plots generated during the procedure of calibration pedestal subtraction training event number. The plot presents mean value of collected ADC counts as a function of number of training events.

4. Conclusion

In this note, the SALT's emulation software has been presented. The all digital processing algorithms are implemented and comprehensively tested. The software platform can also make tuning of the run parameters. This software will be a crucial part of the maintenance of the future tracking LHCb's detectors.

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