THE ALFA TRIGGER SIMULATOR*

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(Received May 4, 2015)

The paper presents basic information about ALFA detectors used in the ATLAS experiment, and the structure of currently developed device used to test a new ALFA trigger interface. It discusses the block diagram of the device, principle of its operation, implementation details and future plans for developing the Simulator.

DOI:10.5506/APhysPolB.46.1271
PACS numbers: 29.50.+v, 07.05.Hd

1. Introduction

ALFA detectors are part of the ATLAS experiment located at the LHC in CERN, Geneva. The aim of ALFA is to measure Absolute Luminosity For ATLAS. To minimize the uncertainties of the luminosity measurements, it is necessary to perform series of tests of detectors, data acquisition system, interfaces and all cooperative systems. The main aim of the ALFA trigger simulator (ATS) is to generate test signals for debugging and commissioning of the newly designed ALFA_CTPIN interface board. This new interface installed for Run2 will allow ALFA detectors to run together with other subdetectors of ATLAS in combined mode, synchronously with the LHC.

* Presented at the Cracow Epiphany Conference on the Future High Energy Colliders, Kraków, Poland, January 8–10, 2015.

2. ALFA detectors

The eight detectors are installed in four stations located on both sides of the ATLAS IP — two stations on each side with two detectors in each station. Stations are located in opposite sides in the LHC tunnel about 240 m from the interaction point. That distance is required for the main aim of measurement — tracking elastically scattered protons under very small angles.

All detectors are located in Roman pots (Fig. 1, left). It gives possibility of moving detectors in the aperture without polluting the vacuum of the beam pipe.

Main detectors (MD) are made of 10 double layers of perpendicular scintillating fibers (Fig. 1, right). MDs are used to track elastically scattered protons. There are also two (in every Roman pot) additional detectors called overlap detectors (OD). ODs are made of 30 fibers per each detector. They are used to align MD detectors when approaching the beam. All scintillating fibers are attached to multianode photomultiplier tubes (MAPMTs) which are connected to front-end boards. Front-end boards convert analog signals from photomultipliers to digital pulses, which are sent to motherboards located in every stations. More details about ALFA experiment are collected in [1].

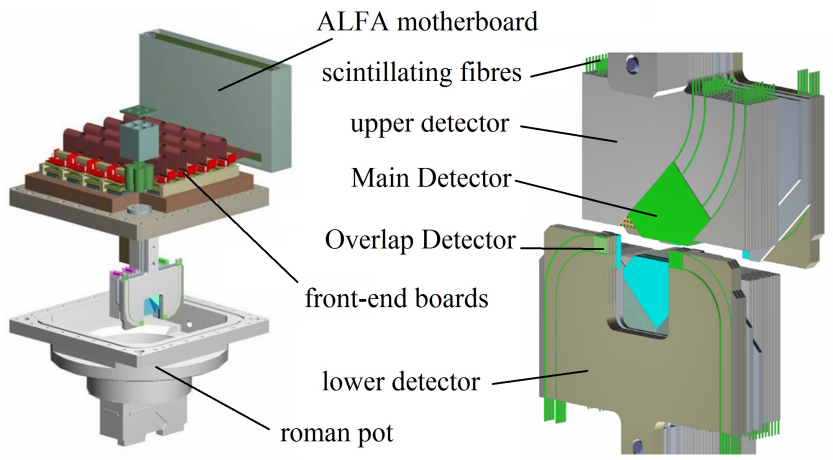

Fig. 1. Scheme of the upper detector with front-end electronics and motherboard in the station station (left) and scheme of upper and lower detectors (right) [1].

There are LEDs installed inside the Roman pots which can be used to illuminate detectors. The LED flashes enter the lightpath at the junction of scintillating fibers and the multianode photomultipliers giving the possibility to test further data path. There is also possibility to test and calibrate front-end boards.

3. Trigger and data acquisition system

The ALFA detectors and all other ATLAS subdetectors running together in combined mode send trigger signals to the CTP (Central Trigger Processor) (Fig. 2). To minimize the time of transmission, triggering signals from ALFA are sent via air-cored cables where the signal speed approaches 91% speed of light. Raw data from the individual events are stored in the trigger L1 pipelines located in the front-end electronics. The CTP analyses trigger signals, and if the combination is interesting for physicists, the CTP generates the L1 accept (L1A) signal. This signal, together with the bunch crossing number and the L1 event number are distributed to all detectors participating in the run via the ATLAS TTC system (Trigger, Timing and Control). The ALFA motherboards send detailed data about events selected by the CTP to readout driver (ROD). Further way of data is the readout system (ROS) and higher triggering levels.

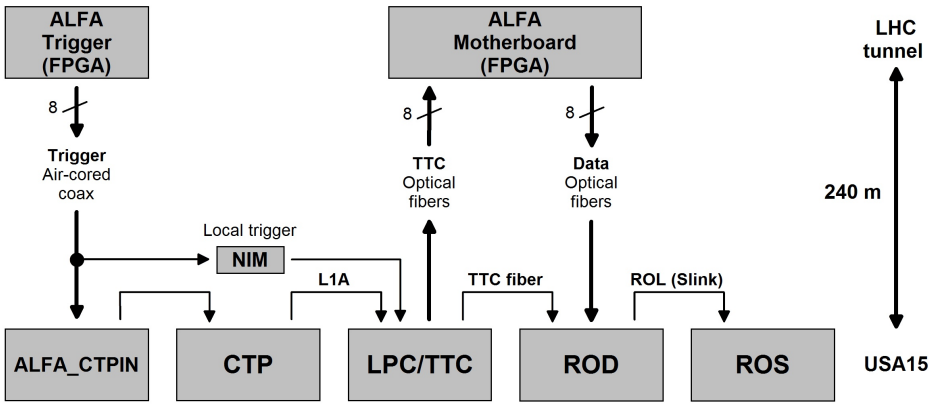

Fig. 2. Diagram of first level trigger [2].

Experience from Run1 shows that it would be desirable to have a common latency for the high luminosity operation and for special ALFA runs. Together with modifications to the CTP for Run2, it was proposed to build a dedicated ALFA trigger interface ALFA_CTPIN to minimize the latency needed for ALFA and which could be used to avoid ATLAS latency changes.

4. Simulating tools and device

The tester that we develop is based on ZedBoard — Zynq evaluation and development kit equipped with Zynq 7020 integrated circuit. Zynq combines microcontroller with dual core ARM processor (two Cortex A9 cores with 800 MHz clock) and FPGA logic (field-programmable gate array).

The microcontroller is used to program memory with desired patterns of the test signals and to communicate with the operator via UART interface and in future plans via Ethernet. The programmable logic generates test signals and synchronizes them with the LHC clock.

The communication with the tester is organized on virtual RS232 (COM) port. It is connected by USB port but the operating system on workstation sees it as a port COM. Via this interface, we send the table of patterns to the microcontroller. The microcontroller analyses the table of patterns and programs block RAM (located in FPGA part of integrated circuit) via port A using AXI4 Lite bus (Fig. 3). The clock wizard synthesizes 80 MHz clock from the input LHC clock of 40 MHz. The faster clock is necessary to simulate 12.5 ns signals from OD. When the simulation is active, the data from block RAM are readout synchronously via port B with 80 MHz synchronous with the LHC clock. The address at port B is generated by the counter running on twice the frequency of the LHC clock and using the LHC ORBIT as reset. Also all programmable logic is synchronized by synthesized LHC clock. The pattern from address pointed by the counter is sent to signal generator.

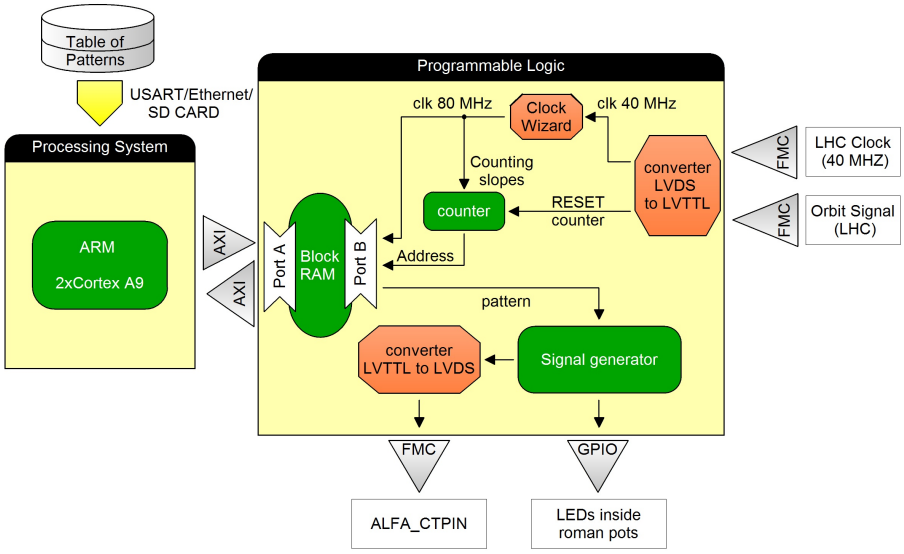

Fig. 3. Block diagram of ALFA trigger simulator.

The signal generator encodes the MD and OD signals by changing the length of the generated pulse: 12.5 ns for the OD and 25 ns for the MD. Signals which are sent to CTP or to LEDs located in Roman pots. The signals generated from the ZedBoard are sent either to the ALFA_CTPIN module or to the LEDs installed in the stations to provoke the detectors

to produce corresponding triggers. ZedBoard signals which are sent to ALPHA_CTPIN need conversion from low voltage TTL (standard of voltage used on ZedBoard) to LVDS (low-voltage differential signaling). The converter is located in Zynq. LVDS signals are sent to the FMC port (located on ZedBoard) which is connected to ALPHA_CTPIN via LVDS to NIM converter. Output signals from NIM converter to ALPHA_CTPIN via LEMO cables are analyzed as signals originating from the ALFA detectors.

The other configuration which is to be used for the ALFA_CTPIN test is based on detector activation by LEDs blinks inside Roman pots. In this test series, we can test all way of signal from scintillating fibers through photomultipliers, front-end boards, motherboards, new ALFA_CTPIN interface up to CTP. This gives a possibility of calibration of front electronics.

Console application is used to configure the test program (Figs. 4 and 5). An user can choose the option by entering its number. Application menu allows the user to program single memory cell or program all memory with

```
nowa 5 ALFA IP test begin.
-------------------------------------------

loading memory via port A
With value: 0


**************************************************
*                                                *
*      ALFA Trigger Simulator v 1.0308 'lady'    *
*                                                *
**************************************************


Main Menu:
Select and check memory cell. . . . . . . . . . 1
Check all memory. . . . . . . . . . . . . . . . 2
Select and change value in memory cell. . . . . 3
Fill all memory with pattern (only main detector):
     401  0x00   |   406  0x55   |   411  seq_1
     402  0xFF   |   407  0x33   |   412  counts
     403  0x0F   |   408  0xCC   |   413  none
     404  0xF0   |   409  0xDD   |   414  none
     405  0xaa   |   410  0x88   |   415  Sune seq
                  Fill with other pattern. . 4
Load precompiled test configuration . . . . . . 5
Start simulation (internal clock) . . . . . . . 6
Start simulation (LHC clock). . . . . . . . . . 7

alfa_led >:
```

Fig. 4. Main menu of ALFA Trigger Simulator in RS232 console application.

a predefined sequence of patterns. After the simulation start, the device is synchronized with LHC clock and ORBIT signals. The simulation is stopped by pressing ENTER key.

```
alfa_led >: 415
Loading memory via port A...
Loading memory finished!


Main Menu:
Select and check memory cell. . . . . 1
Check all memory. . . . . 2
Select and change value in memory cell. . . . . 3
Fill all memory with pattern (only main detector):
     401  0x00   |   406  0x55   |   411  seq_1
     402  0xFF   |   407  0x33   |   412  counts
     403  0x0F   |   408  0xCC   |   413  none
     404  0xF0   |   409  0xDD   |   414  none
     405  0xaa   |   410  0x88   |   415  Sune seq
                     Fill with other pattern. . 4
Load precompiled test configuration . . . . . 5
Start simulation (internal clock) . . . . . 6
Start simulation (LHC clock). . . . . 7

alfa_led >: 2

Print memory:
address: 0    BCX: 0    value: mmmmmmmm.
address: 1    BCX: 1    value: --------.
address: 2    BCX: 2    value: --------.
address: 3    BCX: 3    value: --------.
address: 4    BCX: 4    value: oooooooo.
address: 5    BCX: 5    value: --------.
address: 6    BCX: 6    value: --------.
address: 7    BCX: 7    value: --------.
address: 8    BCX: 8    value: momomomo.
address: 9    BCX: 9    value: --------.
address: a    BCX: 10    value: --------.
address: b    BCX: 11    value: --------.
address: c    BCX: 12    value: m-------.
address: d    BCX: 13    value: -m------.
address: e    BCX: 14    value: --m-----.
address: f    BCX: 15    value: ---m----.
address: 10    BCX: 16    value: ----m---.
address: 11    BCX: 17    value: -----m--.
address: 12    BCX: 18    value: ------m-.
address: 13    BCX: 19    value: -------m.
address: 14    BCX: 20    value: o-------.
```

Fig. 5. Listing of first few memory cells in RS232 console application. In value field, there is a pattern which the simulator sends to CTP. "m" means event in Main Detector, "o" — Overlap Detector, "–" — no event.

5. Future plans

Simple preliminary tests of our tester have been run at CERN. We continue to work on further development of our device taking into account the guidance sent from the ALFA staff.

In near future, we want to install Linux operating system on the ZedBoard. It will make our device independent from the COM port on the workstation. It will also add new possibilities to configure new test patterns. Moreover, it creates a possibility of a remote control of our device via LAN and the Internet (SSH protocol). We also work on application with graphical user interface with table of pattern wizard.

6. Summary

The main aim of this project is a design and development of device used to test new interface between ALFA detectors and CTP. To test the interface, our tester uses the table of patterns containing special prepared patterns. There are two ways of testing. First, user can send signals directly to ALPHA_CTPIN from simulator as the signals from detectors, and other one — by excitation the detectors with LEDs blinks located inside of Roman pots.

REFERENCES

[1] B. Allongue *et al.*, *JINST* **7**, C02034 (2012).

[2] K. Korcyl, "ALFA detector: timing and trigger", Proc. of SPIE Vol. 8903 89032K-1.