SIMULATION OF UPSTREAM TRACKER DETECTOR RESPONSE FOR MODERNISED LHCb EXPERIMENT*

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LHCb experiment operates a forward spectrometer that collects proton–proton collision data at the Large Hadron Collider at CERN. During the so-called Long Shutdown 2 period in years 2018–2019, LHCb detector will undergo a major modernisation. A vital part of this upgrade process is building a silicon micro-strip tracking detector — Upstream Tracker (UT) — that will be placed before the bending magnet. The UT will play a critical role in the upgraded trigger system. This paper contains a general discussion of the UT detector and presents description of a silicon response simulation platform that is being currently designed by the AGH UST LHCb group.

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1. Introduction

The Large Hadron Collider beauty (LHCb) is an experiment dedicated to explore the imbalance between matter and antimatter in the Universe. It is a forward spectrometer corresponding to a range of $2 < \eta < 5$ units of pseudorapidity where we expect to observe a copious production of hadronic particles containing beauty and charm quarks. Studying these particles is the best way for examining CP violation in the Standard Model and for searching signals of the New Physics. The LHCb experiment will undergo modernisation in years 2018–2019 in order to provide full detector readout at the LHC bunch crossing rate and to allow its operation at a constant instantaneous luminosity of 2×10^{33} cm^{-2}s^{-1}.

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2. Upstream Tracker

The Upstream Tracker is a silicon micro-strip tracking detector, which will replace the Tracker Turicensis (TT) detector, that is being used in the current LHCb experiment. The location of the TT detector in the LHCb spectrometer is shown in figure 1.

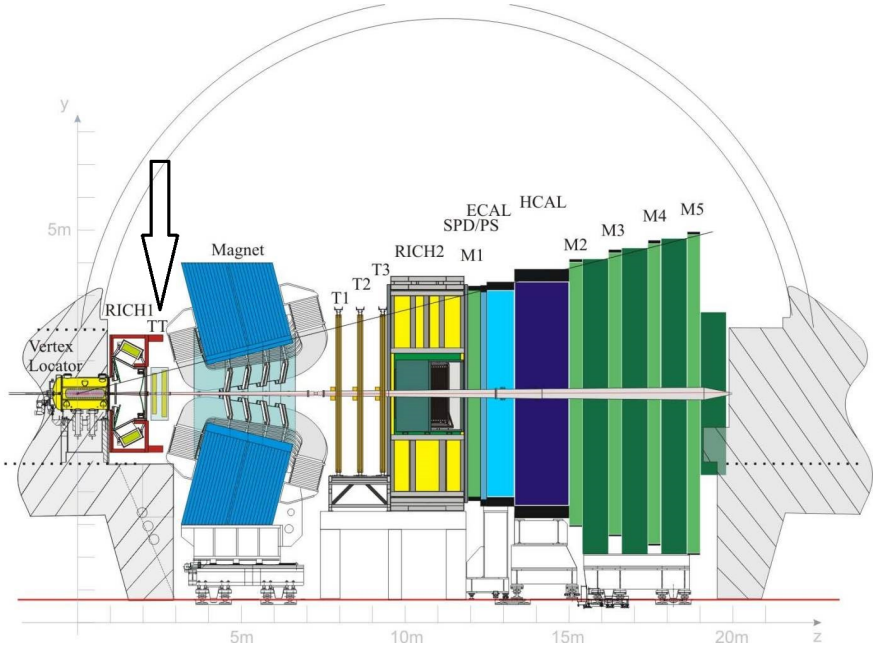


Fig. 1. Layout of the LHCb spectrometer. The arrow indicates the TT detector [1].

The upgraded LHCb experiment will consist of improved subdetectors, however it will maintain its current geometry. The Upstream Tracker will play a crucial part in the track reconstruction of particles decaying after the Vertex Locator (VELO) detector and particles bended out of the acceptance region by a magnet (so-called upstream tracks, see figure 2).

A consequence of absence of the magnetic field in the VELO region is the fact that VELO-only tracks have no momentum information. Yet, tracks measured both with the UT and VELO detectors will have 15% momentum resolution, moreover tracks extended to the SiFi detector will measure momentum with 0.5% resolution. Furthermore, use of the UT will significantly reduce an execution time of the track reconstruction in the modernised LHCb experiment [3].

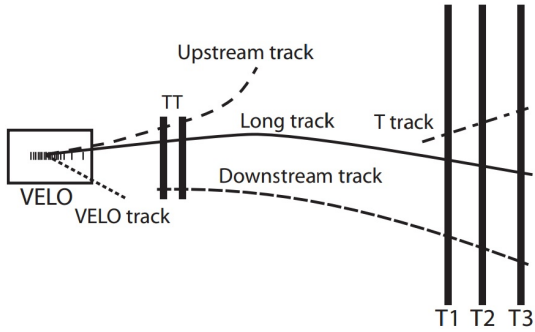


Fig. 2. Track definitions as used by the LHCb Experiment [2].

The Upstream Tracker will have many features in common with the Trigger Tracker (*e.g.* the UT like the TT will consist of four sensors layers, sequentially rotated relative to each one about 0°, −5°, +5°, 0° — showed in figure 3).

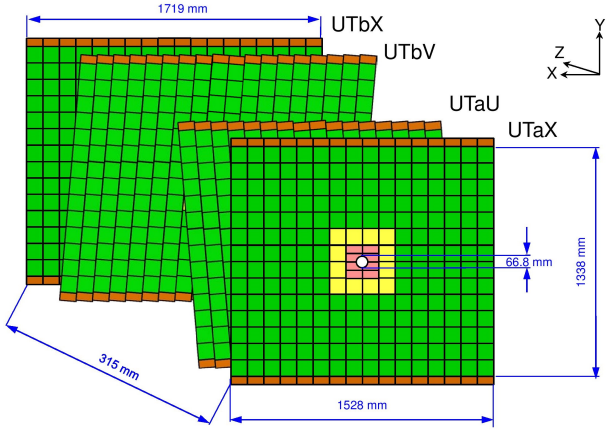


Fig. 3. Scheme of four sensor layers in the UT detector [5].

2.1. Data flow in the simulation sequence

A good starting point for the process of developing algorithms for the simulation of the UT detector is to partially use the code designed for the TT because of similarity between these two detectors.

Current algorithms used for the simulation of the Tracker Turicensis create the following sequence in the LHCb digitization application:

— MCSTDepositCreator,

— MCSTDigitCreator,

— STDigitCreator,

— STClusterCreator,

— STClusterKiller,

— STClustersToRawBankAlg.

The general idea of the silicon tracker response simulation can be divided into three parts. The first three algorithms in the simulation sequence correspond to the part responsible for a simulation of a physics in a silicon and an emulation of noises due to an electronics operation which is built in the detector. Then, fourth and fifth algorithms correspond to the part responsible for processes of clusterisation and removing dead clusters. Last but not least, the STClustersToRawBankAlg algorithm simulates a transport protocol.

The first object entering this simulation sequence is a final result of a Monte Carlo (MC) simulation of proton–proton collisions inside the LHC, produced in the LHCb simulation application used for production of different types of particle event, which is based on the Pythia and the EvtGen generators and the GEANT4 toolkit. Such an object contains all possible information about a particle entering the detector. An outcome from a complete simulation sequence is a data set with information about a detector response, which is used afterwards for further processing, *i.e.* for the tracks reconstruction. After this part, one have complete MC samples used for data analysis, so without the UT part in the simulation, it will not be possible to analyse any data collected after planned modernisation. Only the silicon charge deposit simulation will maintain its present architecture on the grounds that the physics in the silicon will not change after the modernisation. The Upstream Tracker detector will have a brand new read-out electronics, which will be reflected in the design of the digitization model. In addition, electronic readout board will be completely replaced so the clusterization and the transport protocol part will be completely different as well [4].

2.2. Silicon ASIC for LHCb Tracking

The Beetle readout chip [6] cannot be used for the modernised UT tracker since it has no digital signal processing capabilities that are required for the new acquisition system, which will perform full detector readout at the LHC

clock rate *i.e.* 40 MHz [7]. So, it is necessary to replace it with another readout chip and this is one of the flagship features of the new silicon detector. The front-end chip SALT (Silicon ASIC for LHCb Tracking) that is currently being designed at the Faculty of Physics and Applied Computer Science AGH UST will substitute the Beetle chip in the upgraded detector.

Performance of the first prototype of the SALT chip will be shortly described in the remainder of this section. SALT chip response in time is presented in figure 4. New readout chip is designed to follow closely the electronics specifications with general LHCb electronics upgrade. Its analogue part will consist of readout 128 channels with low power consumption of 1–2 mW. It will also have to have very fast signal integration and its output signal should have the shortest possible tail. The shorter the tail is, the smaller remainder value is *i.e.* the smaller spill-over effect[1] is seen. The remainder (R) is a ratio between a signal value 25 ns after the peak and the maximum signal value.

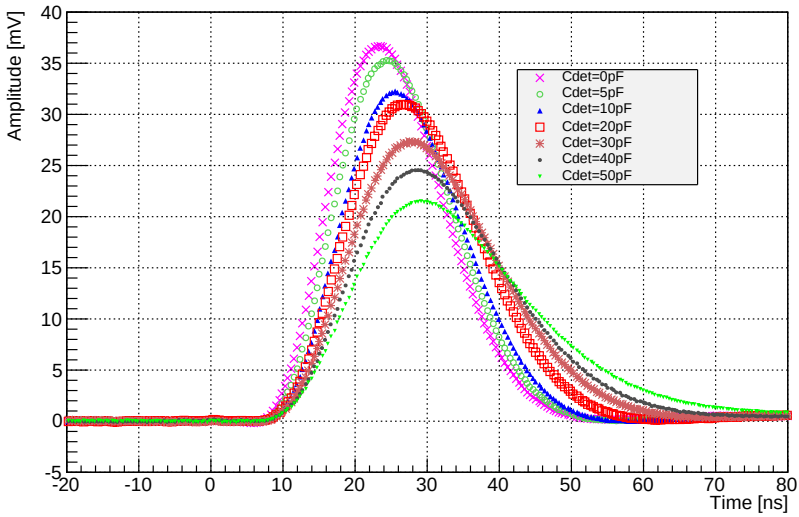
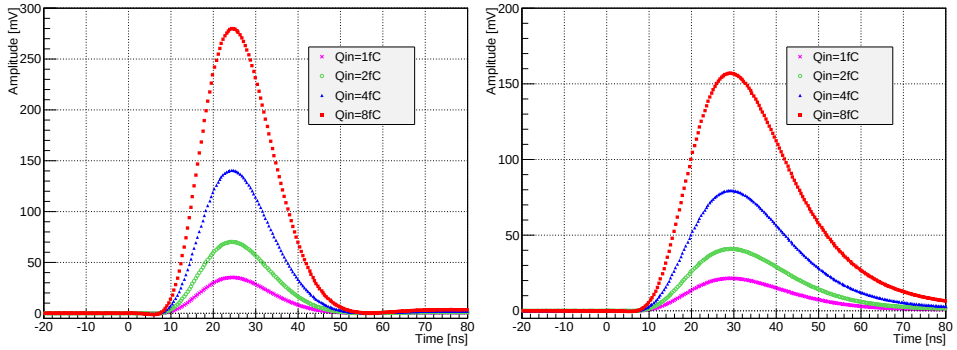


Fig. 4. SALT response as a function of time for the injected charge $Q_{\text{in}} = 1$ fC for variety of capacitences.

In figure 5, on the left, it can be seen a chip response as a function of time for four different injected charges, for a given detector capacitance of 5 pF and in Fig. 6, on the left, there is the corresponding remainder (which is less than 5%). In the same figures, on the right, there can be seen analogous plots for 50 pF. A pulse shape for 50 pF is an extreme example

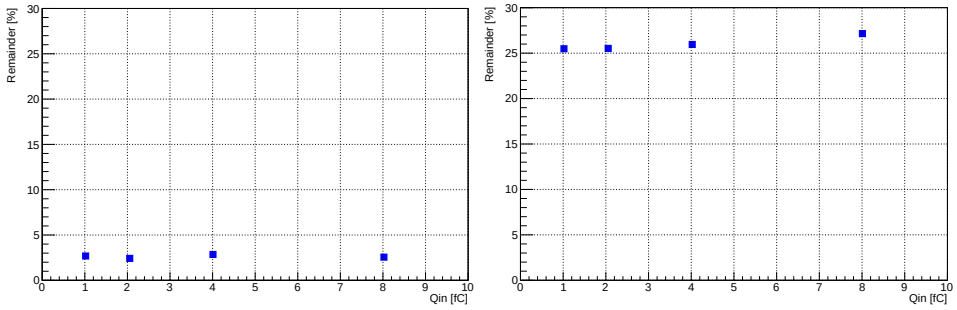
[1] Spill-over effect happens when the residue of the previous signal overlaps with the current signal.

(expected capacitanses in the UT vary between 5–20 pF) and even for such a big detector capacitance, the remainder of a peak voltage is less than 30% (such a requirement had the Beetle chip).



(a) $C_{\mathrm{det}} = 5$ pF (b) $C_{\mathrm{det}} = 50$ pF

Fig. 5. SALT response as a function of time for the given detector capacitances (C_{det}) for variety of injected charges (Q_{in}).



(a) $C_{\mathrm{det}} = 5$ pF (b) $C_{\mathrm{det}} = 50$ pF

Fig. 6. Remainders as a function of injected charge for the detector capacitances (C_{det}).

Figures 7 and 8 show a dependency of the SALT response as a function of a detector capacitance and an injected charge, for a given time of 26 ns (close to average value of the signal raising time). Both dependencies are not constant. It should be noted that in order to emulate SALT response in the UT simulation, it is necessary to consider this behavior.

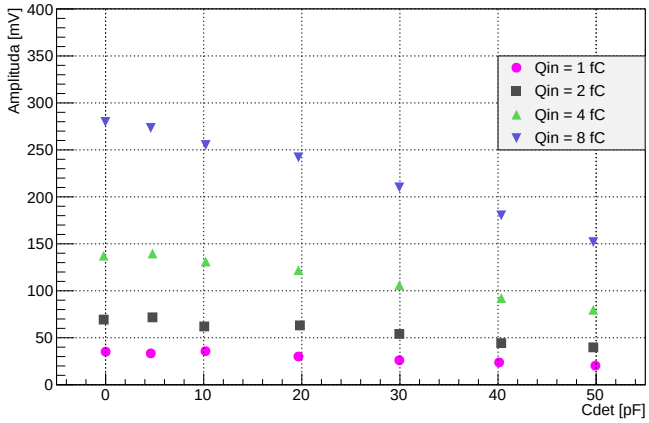


Fig. 7. SALT response as a function of a detector capacitance for a given time of 26 ns.

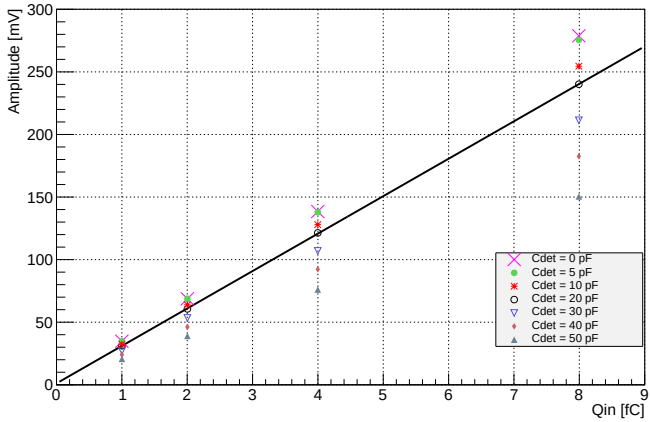


Fig. 8. SALT response as a function of an injected charge for a given time of 26 ns.

3. Summary

A general idea for the UT simulation has been described. The Upstream Tracker will be a critical element in the LHCb modernisation during LHC shutdown in years 2018–2019. It is a silicon micro-strip detector that will replace the Tracker Turicensis in the current LHCb experiment in order to meet the LHCb upgrade specifications (*e.g.* full detector readout at the LHC bunch crossing rate and ability to work at instaneous luminosity of 2×10^{33} cm^{-2}s^{-1}). The crucial part of the UT detector is its readout chip SALT — designed at the AGH University of Science and Technology. Currently, algorithms for the simulation of the UT detector response are under development.

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