SOFTWARE PLATFORM FOR THE MONITORING AND CALIBRATION OF THE LHCb UPGRADE I SILICON DETECTORS*

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Run 2 of the proton–proton collision data taking has finished at the end of 2018 and is now followed by the second long shutdown period (LS 2) that is going to be used for various upgrades and modification of all experiments operating at the LHC machine. The LHCb experiment will undergo a major upgrade in that time. In particular, the whole charge particle tracking system will be exchanged and adapted to read-out data at the LHC machine clock (40 MHz). Silicon planar technologies will be used for the vertex detector and Upstream Tracker. In this paper, we report on current status and plans regarding preparation of the high-level software platform for the emulation and monitoring of the silicon detectors of the upgraded LHCb spectrometer. This software is going to be an essential part of both detectors commissioning and daily operation.

1. Introduction

The LHCb (Large Hadron Collider beauty) [1] is a dedicated flavour experiment optimized to studying CP (charge-parity) violation in heavy quark sector and searching for new physics phenomena. Its entire physics programme relies on a high-precision tracking system. During the LS 2, the spectrometer will be modernized to allow it to operate at five times higher instantaneous luminosity (with respect to the luminosity during Run 2) and cope with much higher particle fluences up to $10^{15}\,n_{\mathrm{eq}}\mathrm{cm}^{-2}$ (n_{eq} — neutron equivalent). A new VELO detector will be based on the hybrid pixel technology, while the Upstream Tracker will feature higher granularity and acceptance in comparison to its predecessor.

The Vertex Locator (VELO) is dedicated to high-precision reconstruction of primary and secondary vertices, the geometrical impact parameter and is essential for life-time measurements. First active pixels are at a distance of 5.1 mm from the proton beams. The large radiation damage effects expected for the new VELO and enormous data rate (900 million hits for the hottest sensors) led to the decision of changing the micro-strip technology [2] to hybrid pixel one [3] with triggerless readout system compatible with the 40 MHz software trigger. The new VELO will contain 26 stations mounted in two separate halves, each station consists of two modules that in turn comprise of 4 silicon pixel sensors. Each such a sensor is read out by 3 VELO ASIC's — Velopix's. Each Velopix is able to handle 256×256 pixels[1]. The schematic view of the new VELO detector is presented in Fig. 1.
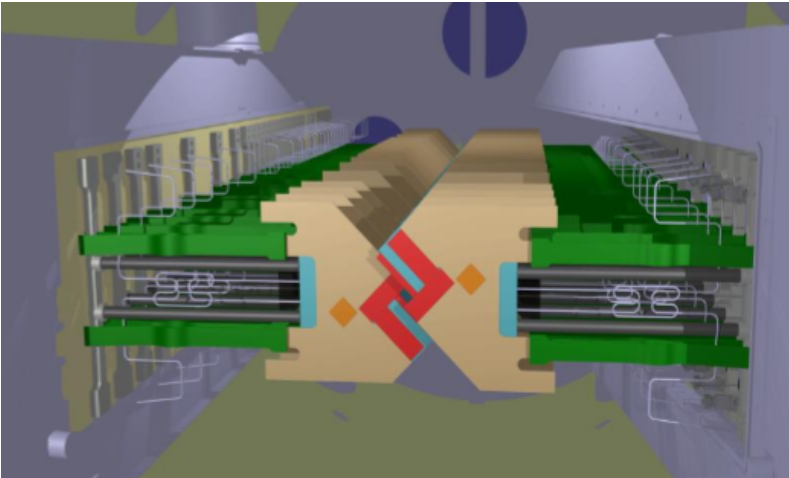

Fig. 1. The new Vertex Locator (VELO) visualized. Sensitive sensor area is up to 5.1 mm to the beam. VELO will consists of 26 stations, each of them containing 4 pixel senors (two on each side) read out by 12 Velopix ASIC's in total.

The second silicon detector that will be a part of the upgrade tracking system is Upstream Tracker (UT). This detector is located behind the VELO and before the dipole magnet. It consists of four measuring planes of silicon micro-strip sensors arranged in a similar manner to the old detector [4]. The schematic view of the UT detector is shown in Fig. 2. The measuring planes are divided into vertical structures called staves. The upstream planes (UTaX and UTaU) are divided into 16 and the downstream (UTbV and UTbX) into 18 staves, respectively. Each stave in turn has fourteen square

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[1] The VELO sensors feature square $55\,\mu\mathrm{m} \times 55\,\mu\mathrm{m}$ pixels.

sensors of 98.88×98.88 mm size, except for the central region, where some of the sensors are half length and some of them have circular cutout allowing to extend the acceptance of the UT up the beam pipe. Strip pitches are 190 μm and 90 μm for the sensors in the outer and inner regions, respectively (consult Fig. 2).
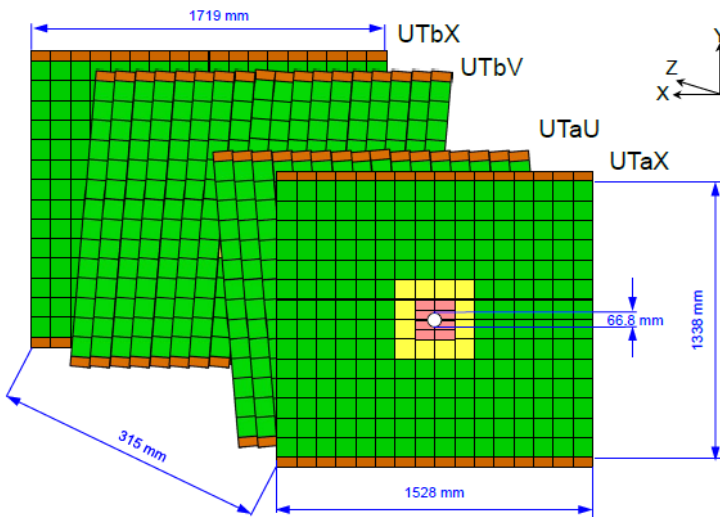

Fig. 2. (Colour on-line) Overview of UT geometry looking downstream. The different sensor geometries are colour coded. The green (outer) sensors have 512 strips with the pitch of 190 μm, the yellow (middle) and red (inner) have in turn 1024 strips with the pitch of 90 μm.

2. Emulation and monitoring software

By the emulation process, we understand the raw data processing implemented in the high-level software that mimics the hardware implemented DSP (Digital Signal Processing) that is performed in the readout electronics on the detector side. The purpose of the emulation is threefold: detailed monitoring of each step of the processing, calibration of the processing algorithms and potential enhancements of the processing of the raw data. In addition, the expected high particle fluencies for the VELO and the inner region of the UT will make the emulation a vital tool in operation of the two silicon systems. In the remainder of this section, a short description of the emulation procedures for the UT (Sect. 2.1) and VELO (Sect. 2.2) are given.

2.1. UT emulation suite

In the case of the UT detector, the signal collected on strips is sampled by a sophisticated analog module of the front-end chip SALT (Silicon ASIC for LHCb tracking) [5], digitized and processed by an integrated DSP block. The processing chain implemented in the SALT chip consists of the following steps: bad channel masking, pedestal subtraction, mean common mode suppression and zero suppression (*cf.* Fig. 3). The last step is performed using a carefully tuned single threshold (called a low threshold), and the output data is encoded and sent for further processing to the electronics acquisition Tell40 boards. The final steps of the processing are the spill-over detection[2] and clusterization. The UT emulation suite must combine both domain (SALT and Tell40) and will play a vital role in processing algorithms testing, tuning (configuration parameters must be determined in a dedicated calibration runs) and monitoring.
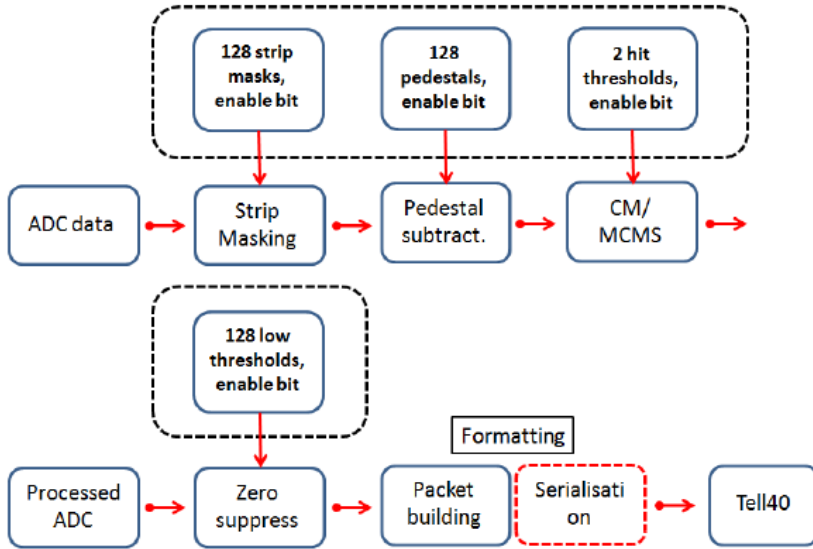
Fig. 3. Baseline digital signal processing chain for the SALT ASIC. Dedicated calibration runs will be used to determine processing parameters for the DSP algorithms configuration.

2.2. VELO emulation suite

This suite is mainly focused on Time-over-Threshold emulation (ToT), basing on simulated or taken by the real detector analog ToT data. Deposit-

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[2] A channel that registered a hit in a previous bunch crossing is excluded from the hit reconstruction in the next bunch crossing using a spill-over flag.

ing charge in the pixel active area leads to injecting equivalent charge to the input of pixel front-end electronics, where the charge is later discharged by a limited constant current, causing the signal to last for a certain time, depending on the quantity of injected charge. The deciding element of signal occurrence at the electronic stage is a comparator — ToT data inform us how many times the comparator triggered a positive result for the last signal seen in each pixel. Activated charge can spread over many pixel's areas, hence the signal response might be seen in many consecutive pixels and not only in a single pixel. If the charge is high enough to cross the voltage threshold, the pixel will light up. To get the entire charge of one specified event, charge from all pixels which participated in the event must be integrated. Integrating of the charge from the pixels is done through clusterization, the procedure that combines all the ToT counts which may come from the same event. This is currently done by the step-by-step algorithm, however, there is a potential to use machine learning techniques, which will improve the performance, similarly to problems in other fields of science, which have introduced some kind of intelligent exploration [7].
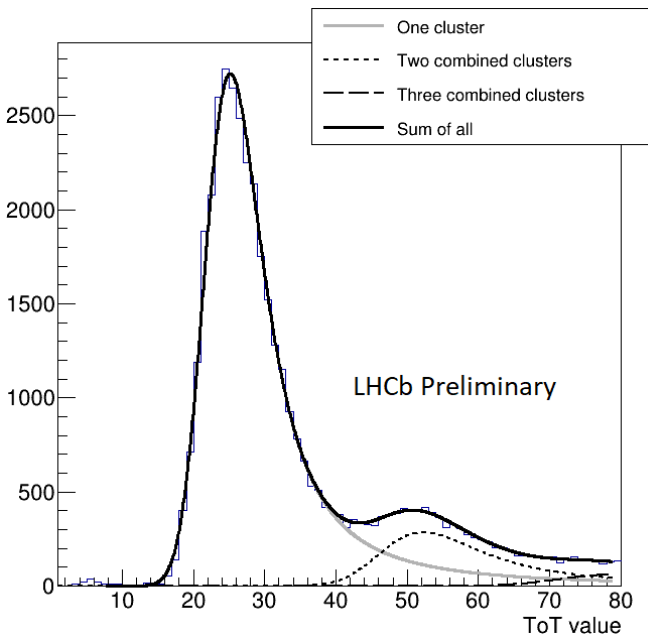

Fig. 4. Exemplary Time-over-Threshold emulation performed on the analog data of Velopix. Full model consists of several parts, in which the data readout system imperfections were included and added to the fit. The one cluster distribution is the pure Landau distribution and precisely corresponds to the charge deposited in the sensor [6].

Since the time of sensor response is proportional to the injected charge, ToT should be proportional to the collected charge. This positive feature allows us to recreate charge distribution basing on ToT data. One of the major disadvantages of ToT data is that clusters can be combined with each other, therefore, the final distribution is a summary of one cluster distribution and consecutive combined distributions. The result based on Velopix measured analog data is presented in Fig. 4.

3. Calibration — pixel equalization

One of the monitoring functionalities is the detector calibration. The calibration of VELO detector is done at the hardware level with a dedicated steering software. Pixels characterizes themselves with two significant calibration properties, a gain and voltage pedestal level. Both parameters depend on a pixel's amplifiers working point, however, voltage pedestal level can be also controlled via an outer-steered parameter called trim. Trim is basically an offset added to the pedestal voltage before the signal comparator checks if the signal is higher or lower than the settled global threshold level value. If voltage is higher, the comparator returns value of 1, which is considered as signal existence. Naturally, calibration of the pixels might have been performed through gain linearization, where baseline voltage would be an offset, yet it is impossible at the hardware level. Hence, the calibration comes down to pixel equalization, the procedure of equalizing the pixels voltage pedestals before the analog comparator stage, neglecting any gain differences. Laboratory measurements shown that voltage pedestal levels are spread over the stretch of around 50 mV. After equalization, where the 4-bit trim value is set to each pixel, pedestal spread is lowered and pixel matrix is equaled, as much as the 4-bit trim value allows. Minor drawback of equalizing pixels in this way is the elevation of all pixel voltage levels, which leads, among others, to an increased power consumption and sensor temperature. Equalization of pixel matrix is performed as follows. Firstly, a threshold scan of voltage pedestal level of each pixel is performed. Since the voltage quantization step of trim is different in each pixel and generally not specified, to each pixel the maximum value of 4-bit trim is added and the quantization step is calculated. Eventually, the optimum trim is designated to each pixel separately, making the total voltage level distribution as narrow as possible. Equalization procedure is visualized in Fig. 5. During threshold scans also information about voltage pedestal fluctuations can be collected, which is crucial to removing participation of damaged pixels with enormous noise, encasing them by a masking bit in a pixel individual memory.
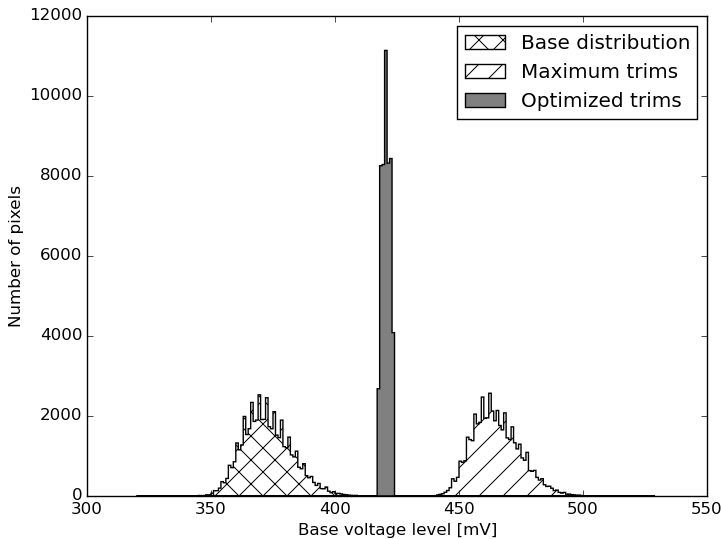
Fig. 5. Equalization consists of three scans, first without adding trims, second with maximal trims, and third with calculated optimized trims. In the end, the equaled distribution (in the middle) is created, where the scatter of voltage pedestals is the lowest.

4. Conclusions

The LHCb Collaboration is preparing a major upgrade of the experimental setup. The tracking system will be a completely rebuilt featuring radiation hard silicon hybrid pixel vertex detector and high-granularity strip tracking stations. The vital part of their daily operation will be related to detailed data quality monitoring, calibration and radiation damage effects studies. Robust and efficient high-level software platform emulating the readout and processing chain is of the utmost importance. Initial implementations for both silicon tracking systems have been provided and will be tested during the upcoming commissioning.

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