GBTX EMULATION FOR BM@N/MPD DATA ACQUISITION SYSTEMS*

Wojciech M. Zabołotny, Adrian Byszuk, Marek Gumiński
Grzegorz Kasprowicz, Michał Kruszewski
Krzysztof Poźniak, Ryszard Romaniuk

Institute of Electronic Systems
Faculty of Electronics and Information Technology
Warsaw University of Technology
Nowowiejska 15/19, 00-665 Warszawa, Poland

David Emschermann, Christian J. Schmidt

GSI-Helmholtzzentrum für Schwerionenforschung GmbH
Planckstraße 1, 64291 Darmstadt, Germany

(Received February 1, 2021)

The GBTX chip is widely used in high-energy experiments. However, due to export restrictions, it cannot be used in NICA. There is significant synergy in building readout chains for CBM and NICA experiments. To fully utilize this synergy, it is important to emulate the essential GBTX functionality in FPGA. For that purpose, the emulator of GBTX (GBTxEMU) has been developed. The GBTxEMU may be implemented in cheap FPGAs, including Artix-7, and enables creating multichannel data acquisition chains based on the same front-end ASICs (SMX2 developed at AGH) as the one used in CBM. The GBTxEMU may work with the DPB boards developed for CBM, but a dedicated, price-optimized solution is under development.

DOI:10.5506/APhysPolBSupp.14.555

1. Introduction

GBTX [1] is a radiation-tolerant ASIC, able to provide multiple high-speed links for high-energy physics experiments. The user data frame with a length of 80 bits (with FEC) or 112 bits (without FEC) is transmitted every 25 ns in both directions via the optical GBT link operating at 4.8 Gb/s data rate. At the Front-end Electronics (FEE) side, this data may be used to

* Presented at NICA Days 2019 and IV MPD Collaboration Meeting, Warsaw, Poland, October 21–25, 2019.

implement so-called E-Links — SPI-like synchronous links, working at clock frequency between 40 and 320 MHz and with data rate between 80 and 320 Mb/s (DDR operation is possible). Additional slow control is possible via a dedicated SCA chip connected to a simple synchronous serial interface.

The GBTX is used in many experiments at CERN and will be used in various detectors in the CBM experiment [2]. A dedicated SMX2 ASIC chip, together with communication protocol, has been developed for GBTX-based readout [3]. The whole system is controlled by FPGA-based Data Processing Boards (DPB) [4].

This GBT-link-based infrastructure may be a good solution for BM@N and MPD experiments prepared at JINR [5]. The GBTX ASIC, however, uses a radiation-hard technology and, therefore, cannot be exported to many countries. That affects the possibility of cooperation at CBM development, and also prohibits its direct usage in MPD and BM@N experiments.

2. GBTxEMU proposal

To enable the development of GBT-link-based readout in all involved institutions and to provide a solution suitable for experiments prepared at JINR, a reimplementation of essential GBTX functionality in the FPGA was proposed[1]. The FPGA implementation is not radiation hard, and that limitation must be taken into consideration when designing the readout system. The project is named GBTxEMU (GBTX Emulator).

The GBTxEMU is supposed to contain just the basic functionalities of the original GBTX without attempting to recreate the full structure of GBTX registers and their functions. To limit the costs, the implementation was aimed at using the chip FPGA family Artix-7. Due to their limited speed, it was planned to drop operation at 160 MHz E-Link clock frequency. It was also considered removing the standard FEC data protection in downlink and replacing it with a simpler equivalent (*e.g.*, triple redundancy with voting). The essential functionality is limited to the distribution to FEE — the jitter-cleaned clock recovered from the GBT link, and simple transfer of data to and from FEE via E-Links. The dynamic control of phase and clock delay in E-links was considered unnecessary. The time-deterministic transmission is required in the downlink direction (to support synchronization of FEE), while a standard non-deterministic latency is acceptable in the uplink direction.

3. GBTxEMU hardware platform

The first GBTxEMU prototype was created based on the TE071-02 module with the TEBA0841-1 baseboard manufactured by Trenz Electronic com-

[1] The first attempt to create such an emulator was made in 2014 [6]. This paper, however, describes a new implementation, based on another architecture.

pany [7]. The control of GBTxEMU was provided by the IPbus interface. However, due to limitations of the platform, a special version for 100 Mb/s Ethernet was developed. That version enabled testing of basic features of the GBTxEMU, including a software-controlled jitter cleaner for clock recovery and communication with a single Front-end Board (FEB) equipped with one SMX2 chip.

Further development was performed using the dedicated GBTxEMU board developed by GSI. The board enables the utilization of integrated Ethernet PHY available in the TE0712-2 module. It provides the hardware jitter cleaner based on the Si5344 chip. It is equipped with two SFP+ cages, enabling IPbus via 1 Gb/s Ethernet or implementation of two GBT links. The board provides also 6 ZIF connectors for the connection of FEE. That version was successfully used for control of multiple FEB boards equipped with 8 SMX2 chips.

4. GBTxEMU firmware

The architecture of the GBTxEMU firmware is shown in Fig. 1. The core component is the GBT-FPGA core originally developed at CERN and modified for use in GBTxEMU. The implementation of the FEC functionality in the downlink direction appeared possible in Artix-7 FPGAs.

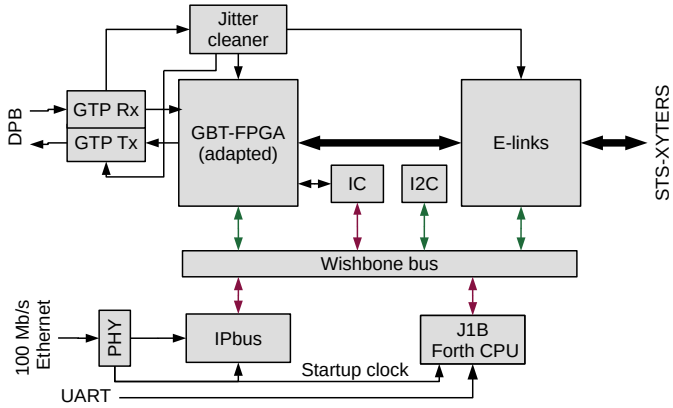

Fig. 1. Block diagram of the firmware of the GBTX emulator.

Another important block is the IP-core, which implements E-Links. Two modes of operation were successfully implemented and tested. With E-Link clock frequency of 40 MHz (data rate 40 Mbps in downlink and 80 Mbps in uplink), 56 E-Links are supported. With E-Link clock frequency of 80 MHz (data rate 80 Mbps in downlink and 160 Mbps in uplink), 28 E-Links are supported. The IP-core also offers limited control of the E-Link clock phase and delay of input data.

The GBTxEMU contains multiple blocks and groups of blocks with internal registers connected to the Wishbone bus. Convenient interfacing them with the software was provided by a specially developed AGWB system [8]. Except for IPbus, the bus may also be controlled by the GBT link, using the Internal Controller (IC). The IC core originally developed at CERN had to be modified to support the bigger address space used in GBTxEMU. The third master of the internal bus is the Forth-based J1B processor [9] that performs the initialization of the GBTxEMU and continuously monitors its operation during normal work. Additionally, it may be used for debugging and diagnostics via the serial UART interface.

5. Results and conclusions

The developed GBTxEMU was successfully used to control FEE via the standard DPB boards with slightly modified firmware. It was possible to control the SMX2 chips in FEE and to transmit the data. Certain modifications of the software layer used to control the DPB boards were necessary, but it is possible to isolate the necessary changes to maintain compatibility between the GBTX and GBTxEMU-based readout chains. The obtained results suggest that GBTxEMU may be a useful component for the development of GBT-based readout chains for applications where the GBTX ASICs are unavailable.

REFERENCES

[1] P. Moreira *et al.*, «GBTX manual», 2018, https://espace.cern.ch/GBT-Project/GBTX/Manuals/gbtxManual.pdf

[2] J. Lehnert *et al.*, *JINST* **12**, C02061 (2017).

[3] K. Kasinski *et al.*, *Nucl. Instrum. Methods Phys. Res. A* **835**, 66 (2016).

[4] W.M. Zabołotny *et al.*, *PoS* **TWEPP2018**, 067 (2019).

[5] P. Kharlamov *et al.*, *EPJ Web Conf.* **158**, 06003 (2017).

[6] S. Mandal *et al.*, *Proc. SPIE* **9662**, 96622Q (2015).

[7] Trenz electronic, 2020, https://www.trenz-electronic.de/en/

[8] W. Zabolotny *et al.*, *Proc. SPIE* **11176**, 1117642 (2019).

[9] W. Zabołotny *et al.*, «Application of Forth CPU for control and debugging of FPGA-implemented systems», presented at XLIV-th IEEE-SPIE Joint Symposium Wilga 2019, https://doi.org/10.13140/RG.2.2.22940.85123