CUSTOM STEP-DOWN DC/DC CONVERTER SYSTEM FOR THE ATLAS ITk STRIP DETECTOR*

Weronika Bulanowska

AGH University of Krakow, al. Mickiewicza 30, 30-059 Kraków, Poland

Received 27 March 2026, accepted 16 July 2026, published online 4 September 2026

An intermediate 48 V to 11 V DC/DC conversion stage, located in Patch Panel 2 (PP2), constitutes a key element of the power delivery chain for the ATLAS Inner Tracker (ITk) Strip detector. The design, based on commercial off-the-shelf components, meets the detector constraints and radiation tolerance requirements. Pre-production DC/DC boards demonstrate efficiencies above 81% across the full load range and low output noise, confirming the robustness of the PP2 system.

DOI:10.5506/APhysPolBSupp.19.5-A2

1. Introduction

As the Large Hadron Collider (LHC) experiments approach the end of their radiation lifetime, preparations for the High-Luminosity LHC (HL-LHC) phase are underway. Within this upgrade program, the ATLAS experiment is developing a new fully-silicon tracking detector, the Inner Tracker (ITk) [1]. The outermost subsystem of the ITk, the ITk Strip detector, will consist of approximately 18,000 strip modules mounted on both sides of the staves and petals, the local support structures in the barrel and endcap regions, respectively.

The strip modules require a stable low-voltage (LV) power supply of 11 V, delivered via dedicated LV lines and locally converted to the operating voltages by on-module DC/DC converters. As shown in Fig. 1, the power delivery chain originates in the service caverns, more than 130 m away from the detector. To reduce ohmic losses in the long supply cables, the system employs a two-stage DC/DC power conversion architecture. The 48 V supplied by the off-detector power supplies is stepped down to 11 V by a DC/DC converter system situated in the regions known as Patch Panel 2 (PP2) within the ATLAS muon spectrometer [2].

* Presented at the 32nd Cracow Epiphany Conference on the Recent Results from Heavy Ion Physics, Kraków, Poland, 12–16 January, 2026.

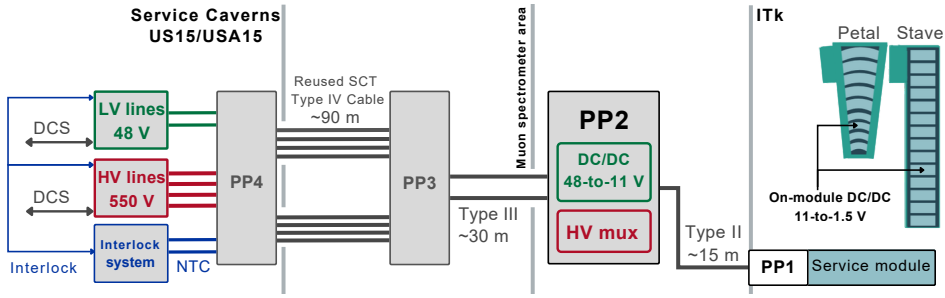

Fig. 1. Power delivery chain for the ITk Strip system. Adapted from Ref. [3].

2. PP2 DC/DC converter system design

The PP2 is a modular, crate-based power distribution system employing the commercial off-the-shelf (COTS) approach to meet the environmental constraints of the ATLAS detector, while maintaining low costs. As shown in Fig. 2, each crate hosts up to twelve insertable DC/DC boards and features a backplane responsible for input/output power distribution as well as routing the communication interfaces between the ATLAS Detector Control System (DCS), the crate controller, and the DC/DC boards.

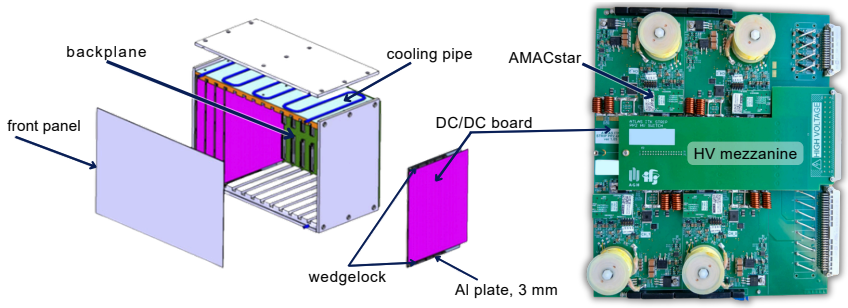

Fig. 2. Left: Schematic of the PP2 crate. Right: Photograph of the pre-production LP board with four DC/DC channels. Adapted from Ref. [4].

Two types of boards are employed: high-power (HP) and low-power (LP), providing a distinct number of DC/DC channels and output current capabilities, with the main parameters summarized in Table 1. The output voltage of each DC/DC channel is controlled by the hardware-based over-voltage protection (OVP) circuitry, which disables the channel if the voltage exceeds the detector electronics safety threshold. In addition, the correction circuitry is implemented to compensate for resistive voltage drops along the supply cables by adjusting the output voltage.

Table 1. Primary parameters of HP and LP DC/DC boards used in the PP2.

Parameter	HP Board	LP Board
DC/DC channels per board	2 channels	4 channels
Detector segment served	Barrel short strip staves	Barrel long strip staves and endcap petals
DC/DC parameters per channel		
Max output current	10 A	5 A
Nominal input current (48 V)	3 A	1.5 A
Output voltage	11–13 V adjustable	11–13 V adjustable

The system design is constrained by harsh operational conditions and integration requirements. Thus, the following solutions are implemented:

— Monitoring and high-voltage (HV) control: Monitoring and control of each DC/DC channel are handled by the AMACstar chip. This ASIC also manages the switching of −550 V HV lines routed through the PP2, switched and split on dedicated HV mezzanines on LP boards.

— Cooling and grounding: Passive cooling is employed via embedded cooling plates. For DC/DC boards, aluminum plates and wedgelocks are used to transfer heat to the crate's cooling system. To avoid ground loops and maintain a single-point grounding scheme, all cooling interfaces and power channels are electrically floating, while signals are routed via galvanically isolated e-links.

— Magnetic field and radiation: To operate in up to 0.6 T magnetic field, conventional ferrite cores are replaced by custom 15 μH air-core inductors. Furthermore, the entire design, including COTS components, is qualified for radiation levels expected in the PP2 region.

3. Radiation tolerance qualification

The radiation tolerance tests were performed according to the ATLAS policy on radiation tolerant electronics [5], with the COTS components selection guided by experience from previous irradiation campaigns, proven technologies, and information available in ESA databases. The irradiation was carried out at the Proteus C-235 proton cyclotron at the Institute of Nuclear Physics in Kraków. A 230 MeV proton beam was used allowing for the simultaneous evaluation of three main radiation effects: total ionizing dose (TID), non-ionizing energy loss (NIEL), and single-event effects (SEE).

The qualification targets were derived from the highest simulated radiation levels (SRL) multiplied by safety factors (SF), as summarized in Table 2, to account for simulation inaccuracies and possible low-dose rate effects. Throughout irradiation, additional SFs of approximately 15 and 2.1 were obtained for TID and SEE, respectively, in order to reach the required NIEL fluence of $5.1{\times}10^{11}$ $n_{\mathrm{eq}}/\mathrm{cm}^2$ (1 MeV neutron equivalent per cm^2). Following irradiation, the components were stored at room temperature for two weeks and subsequently annealed for one week at a temperature of 95°C.

Table 2. Radiation qualification targets for PP2 COTS components. SEE fluence is expressed in terms of hadrons with energy above 20 MeV per cm^2 (h/cm^2).

Effect	Derivation (SRL × SF)	Target	Delivered
TID	15 Gy × 1.5	22.5 Gy	350 Gy
SEE	5×10^{10} $\mathrm{cm}^{-2} \times 3$	1.5×10^{11} h/cm^2	3.2×10^{11} h/cm^2
NIEL	2.6×10^{11} $\mathrm{cm}^{-2} \times 1.95$	5.1×10^{11} $n_{\mathrm{eq}}/\mathrm{cm}^2$	5.1×10^{11} $n_{\mathrm{eq}}/\mathrm{cm}^2$

The irradiation campaign included 12 COTS component types used in the pre-production design including devices employed in OVP circuitry, switching stages, and auxiliary voltage regulation. For each COTS component type, 10 or 12 samples from a single controlled lot were procured and characterized at three stages: before irradiation, shortly after irradiation, and after high-temperature annealing. Figure 3 shows an exemplary characterization result for the gallium nitride (GaN) TP65H480G4JSG transistor [6] used in the HV switching stage.

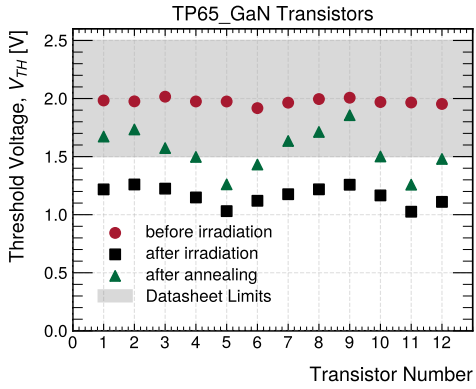

Fig. 3. Threshold voltage at three characterization stages for TP65H480G4JSG GaN transistors. Shaded area indicates manufacturer's datasheet limits.

After irradiation, the threshold voltage of the GaN transistors decreases from approximately 2 V to 1.1 V, and partially recovers after annealing. Despite the parameter shift, the devices remained operational and compliant with the system requirements. Similarly, all observed effects for the remaining COTS components were anticipated and accounted for in the design, with no SEE detected. Results confirmed the radiation tolerance of the selected components for operation in the PP2 environment.

4. Performance of the PP2 DC/DC boards

Pre-production tests of the PP2 system included unit tests on a batch of 44 LP and 18 HP DC/DC boards, independent HV mezzanines tests, and system integration tests, with the former discussed hereinafter.

The power conversion efficiency of the fully assembled DC/DC boards, including losses in the auxiliary circuits, is shown in Fig. 4. The efficiency remains well above 81% for HP and 86% for LP boards across the full-load range. The slightly larger spread observed for LP boards is attributed to minor differences in efficiency between individual channels. Regarding OVP, the mean threshold was measured at 12.9 V with a standard deviation below 50 mV, demonstrating consistent behavior across all LP and HP channels.

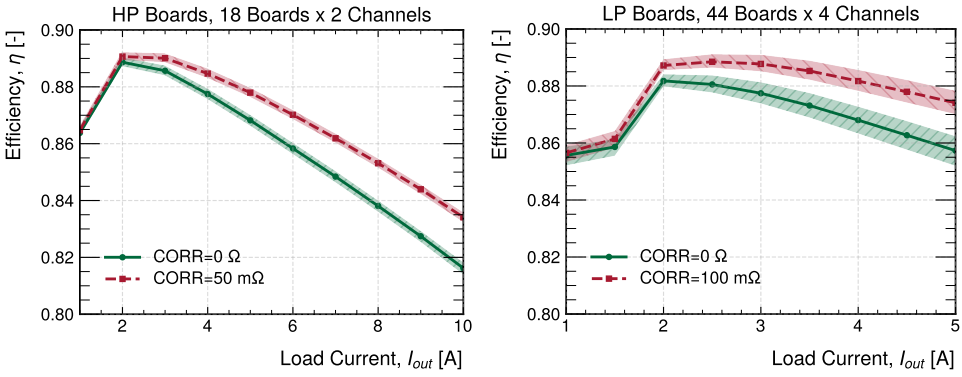

Fig. 4. Power conversion efficiency as a function of load current for 36 HP (left) and 176 LP (right) DC/DC channels. Solid curves show the results without correction, while dashed curves include the correction for expected cable resistance. Curves and shaded envelopes indicate the mean and standard deviation, respectively.

The output noise was characterized at maximum load (given in Table 1) in both common-mode (CM) and differential-mode (DM) configurations, with 50 Ω termination applied to the measurements. The CM noise root mean square (RMS) voltage typically ranges between 5–11 mV for HP boards and 4–6 mV for LP boards, while DM noise RMS remained below 14 mV.

Figure 5 shows the distribution of the output DM and CM noise RMS values for both HP (left) and LP (right) boards, demonstrating low noise levels and uniform behavior across the channels.

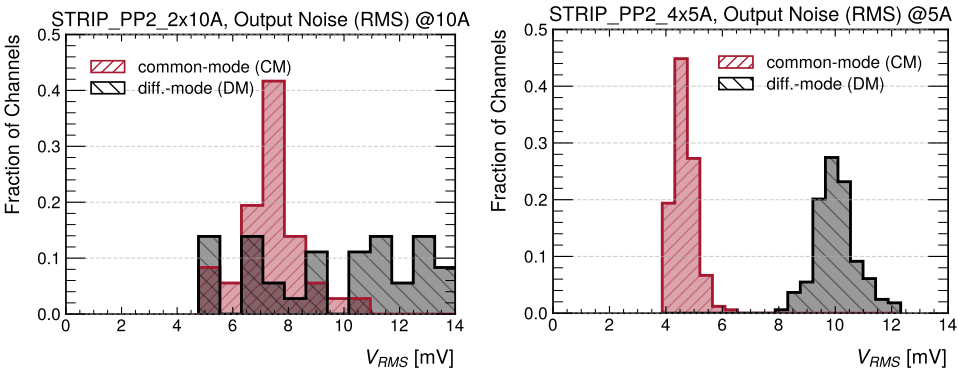

Fig. 5. Distribution of output DM and CM noise RMS values for HP (left) and LP (right) DC/DC channels, measured at maximum load.

5. Conclusions

The pre-production PP2 DC/DC converter system has been characterized and validated. All COTS components demonstrated compliance with radiation tolerance requirements. The DC/DC boards showed high efficiency, reliable OVP, and low output noise under maximum load conditions, confirming the robustness of the PP2 design for full-scale production.

The project was supported by the Polish Ministry of Science and Higher Education, grant No. 2024/WK/07.

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