DEVELOPMENT OF PACIFIC++ FRONT-END ASIC FOR MIGHTY-SCIFI AND MAGNET STATION DETECTOR IN LHCb UPGRADE II EXPERIMENT*

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A successor to the PACIFIC front-end ASIC, currently used in the LHCb Scintillating Fibre (SciFi) Tracker, is being developed for the second foreseen upgrade of the LHCb experiment. The new ASIC, referred to as PACIFIC++, is implemented in 65 nm CMOS technology and extends the architecture of the existing PACIFIC, designed in 130 nm CMOS technology. The new design introduces a 10-bit ADC and a 6-bit TDC measurement in each channel, together with on-chip clustering. The PACIFIC++ is proposed for the readout of the Mighty SciFi Tracker and Magnet Station detectors in the LHCb Upgrade II. An 8-channel prototype version of PACIFIC++, called PACIFIC+8, including all key functionalities, is currently being prepared for submission. This paper discusses the PACIFIC++ architecture and its current state of development.

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1. Introduction

A second major upgrade of the LHCb experiment [1] is planned in order to fully exploit the physics potential of the High-Luminosity Large Hadron Collider (LHC). In the LHCb Upgrade II, the current Scintillating Fibre (SciFi) tracker will be replaced by the Mighty Tracker, consisting of an inner monolithic pixel detector called Mighty-Pixel and an outer upgraded scintillating fibre detector, referred to as Mighty-SciFi. In addition, a new tracking station, called Magnet Station (MS) [2], is proposed to be installed on the magnet side walls.

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The increased luminosity and particle occupancy expected in the Upgrade II environment impose significantly more demanding requirements on the readout electronics. In particular, the readout system for the Mighty-SciFi tracker and the Magnet Stations must provide fast signal processing, precise amplitude and time measurements with efficient data handling in a multi-channel system.

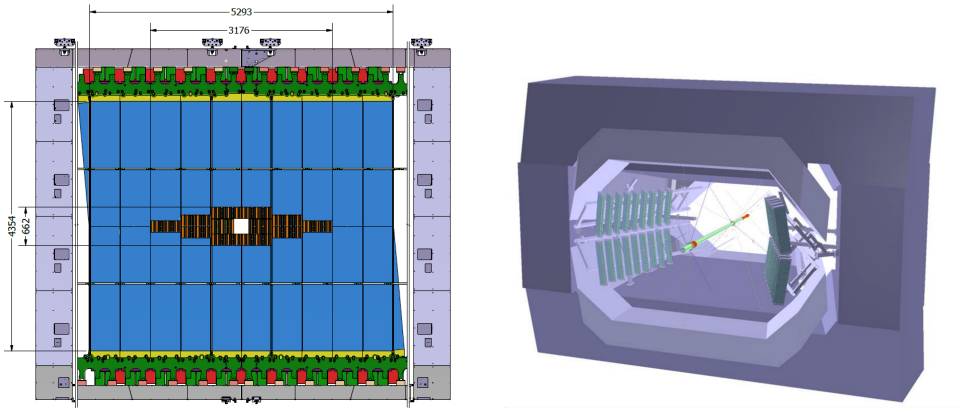
To address these challenges, a new dedicated front-end Application-Specific Integrated Circuit (ASIC) is being developed for the readout of the Mighty-SciFi and Magnet Station detectors. The design is based on the PACIFIC front-end ASIC [3], currently used in the LHCb SciFi detector. The successor ASIC, referred to as PACIFIC++, extends the previous architecture with additional functionalities required for the Upgrade II detectors.

2. Detectors' requirements

2.1. Mighty-SciFi tracker

The Mighty Tracker (MT) consists of three tracking stations and provides essential information for track reconstruction and precise momentum measurement. The outer region of the MT is instrumented with a scintillating fibre detector, referred to as Mighty-SciFi, while the inner region is based on silicon pixel detector technology and is localized in the area of the highest particle rates.

The Mighty-SciFi detector, shown in Fig. 1 (a), will be equipped with scintillating fibres of 0.25 mm diameter, connected to 524 288 channels of Silicon photomultipliers (SiPM), and read out by 8192 newly developed



(a) (b)

Fig. 1. Tracking detectors considered for the PACIFIC++ readout: (a) the Mighty-SciFi tracker [1] and (b) the Magnet Station detector [2].

PACIFIC++ front-end ASICs. The large number of channels and the high hit rates expected in the Upgrade II environment impose stringent requirements on the front-end electronics.

The front-end ASIC must provide fast analog signal processing compatible with the 25 ns bunch crossing window, together with high-resolution amplitude measurement and digitization. In addition, precise time measurement with sub-nanosecond resolution is required to suppress background contributions. Low power consumption is a critical constraint due to the high channel density.

Since the SiPM channels are not aligned with the scintillating fibres and due to the angle of incidence of charged particles, the light signal generated in a fibre is distributed over multiple readout channels. For this reason, on-chip clustering and zero suppression are required in order to reconstruct the hit position efficiently and to reduce the data volume before transmission.

2.2. Magnet Station detector

The Magnet Station (MS), shown in Fig. 1 (b), is a scintillator-based tracking detector proposed to be installed on the magnet side walls. Its role is to provide measurements of the positions and directions of particles traversing the magnetic field, thereby improving the momentum resolution for tracks.

The MS consists of 36 detector modules connected to 55 296 SiPM channels and read out by 864 PACIFIC++ ASICs. The readout requirements are similar to those of the Mighty-SciFi detector in terms of amplitude and time measurement, while on-chip clustering is not required. The front-end electronics must, however, tolerate local hit rate hotspots. The expected hit occupancy is around 0.5% in high-luminosity proton–proton collisions and can reach up to 20% in central PbPb collisions [2].

The inclusion of the MS significantly extends the acceptance towards very low particle momenta. It enables the reconstruction of low-p_{T} particles and improves the mass and momentum resolution for rare events in the presence of large backgrounds.

3. Design of PACIFIC++

The PACIFIC++, presented in Fig. 2, is a 64-channel front-end ASIC developed in CMOS 65 nm technology with precise time and amplitude measurements. Each PACIFIC++ channel includes a fast analog front-end optimized for operation at the 25 ns bunch crossing window. The current signal from the SiPM is converted to voltage by a preamplifier and processed in parallel by the amplitude and time measurement paths, as illustrated in Fig. 2.

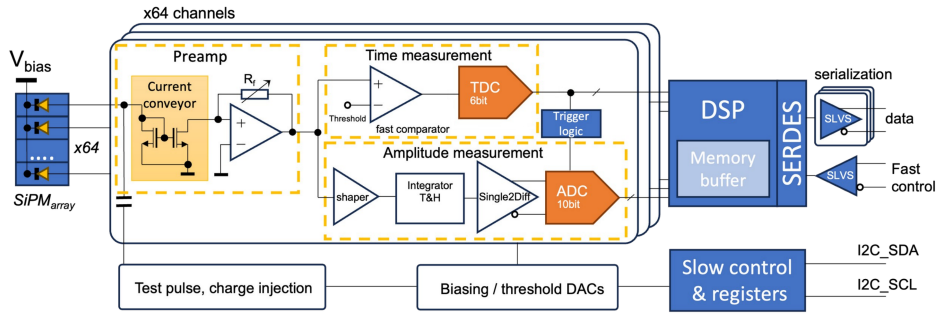


Fig. 2. Block diagram of the PACIFIC++ front-end ASIC architecture.

The amplitude measurement path consists of a shaping stage followed by double-gated integrators, enabling continuous signal processing without dead time. The integrated signal is digitized by a fully differential 10-bit Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) [4] operating at 40 MSps. The full 10-bit resolution is mainly used during calibration procedures, allowing for precise baseline determination and threshold setting in the presence of background signals from irradiated SiPMs. In addition, the amplitude measurement allows for partial identification of particles using $\mathrm{d}E/\mathrm{d}x$ information. In standard operation, amplitude measurement requires only a few bits, typically between 2 and 5.

Time measurement is performed using a fast dynamic comparator connected to a 6-bit Time-to-Digital Converter (TDC). The achieved time resolution of 390 ps is sufficient for precise hit timing and background suppression. The final operating mode of the ADC and TDC is still under evaluation. Currently, two options are being considered: continuous operation, mainly during calibration, or a mode in which the ADC is triggered only by a hit, which allows for reduced power consumption during standard operation.

The Digital Signal Processing (DSP) includes common-mode subtraction, zero suppression, and on-chip clustering. This on-chip functionality is not ready yet, but it will be based on the proven clustering algorithm already employed in the SciFi detector, previously performed outside the ASIC. The on-chip clustering is required for efficient hit position reconstruction in the Mighty-SciFi detector, instead of Field Programmable Gate Array (FPGA) used for the previous PACIFIC readout. The processed data are transmitted off-chip via high-speed serial e-links operating at 1.28 Gbit/s.

The main differences between the PACIFIC and PACIFIC++ designs are summarized in Table 1.

Table 1. Comparison of the main parameters of the PACIFIC and PACIFIC++ front-end ASICs.

Parameter	PACIFIC [3]	PACIFIC++
Technology	CMOS 130 nm	CMOS 65 nm
Number of channels	64	64
Gain	4 selectable gains	8 selectable gains
Sensor bias	Adjustable	None
Power consumption	0.5 W	< 0.75 W
Amplitude measurement	Multi-threshold (3)	10-bit ADC [4]
Time measurement	None	6-bit TDC
DSP	None	Clustering
I/O interface	16 SLVS @ 320 MHz	e-links @ 1.28 Gbit/s

4. 8-channel prototype

The development of the PACIFIC++ ASIC is currently focused on an 8-channel prototype, referred to as PACIFIC+8. The purpose of this prototype is to validate the main building blocks of the final 64-channel design, including the analog front-end, ADC and TDC.

The design of the key functional blocks of the PACIFIC+8 prototype is well advanced. The 10-bit SAR ADC and the TDC have been completed, while for other parts, the schematic design is finished and the layout is currently in progress. The PACIFIC+8 prototype will allow for comprehensive characterization of the full channel performance, including power consumption, timing and amplitude resolution, and other new functionalities. The experience gained with this prototype will be used to optimize the design of the 64-channel PACIFIC++.

The submission of the PACIFIC+8 prototype for fabrication is foreseen for April–July 2026. Following the prototype validation, a first full-size version of the PACIFIC++ is planned, to be followed by a second iteration including all digital features, clustering in particular. This step will lead to the final design and the subsequent mass production phase of the PACIFIC++ ASIC, expected to be completed by 2030, as illustrated in Fig. 3. The later construction and installation phases shown in the timeline correspond to the overall detector project rather than the PACIFIC++ development itself.

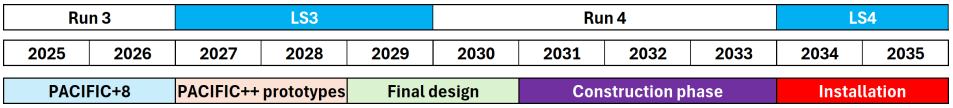


Fig. 3. Development timeline of the PACIFIC++ ASIC, including the PACIFIC+8 prototype, subsequent full-size versions, and the planned production phase.

5. Summary

The Upgrade II of the LHCb experiment introduces new requirements for the readout electronics of the Mighty-SciFi and Magnet Station detectors, driven by the increased luminosity and hit occupancy. The front-end electronics must operate at high speed while providing precise amplitude and time information with low power consumption.

To address these challenges, a 64-channel front-end ASIC, referred to as PACIFIC++, is being developed in CMOS 65 nm technology. The ASIC features a fast analog front-end with per-channel amplitude and time measurements, followed by advanced DSP, including on-chip clustering and high-speed data transmission, to efficiently handle the expected data rates.

The design of the PACIFIC+8, the first 8-channel prototype of the PACIFIC++, is currently at an advanced stage. The prototype is expected to be submitted for fabrication within a few months and will serve as a validation step towards the final full-size PACIFIC++ design.

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