DEVELOPMENT OF FAST TRANSCEIVER FOR SERIAL DATA TRANSMISSION IN LUMINOSITY DETECTOR AT FUTURE LINEAR COLLIDER*

Jakub Moroń†, Mirosław Firlej, Marek Idzik

Faculty of Physics and Applied Computer Science
AGH — University of Science and Technology
Mickiewicza 30, 30-059 Kraków, Poland

(Received January 31, 2011)

A prototype transceiver ASIC for fast serial data transmission in luminosity detector (LumiCal) at the future International Linear Collider (ILC) was designed and fabricated in the AMS 0.35 μm technology. The purpose of the design was to develop a transceiver allowing serial readout of LumiCal detector data up to a highest possible frequency and working in a wide frequency range. The designed ASIC comprises both the transmitter and the receiver circuits. Preliminary measurements showed that both circuits are fully functional and reach the data transmission rates up to about 1 Gb/s. This work presents the transceiver design and the results of preliminary measurements.

DOI:10.5506/APhysPolBSupp.4.41
PACS numbers: 85.40.–e, 29.85.Ca

1. Introduction

An efficient data transmission, *i.e.* the highest rate obtained with the minimum volume of cabling and with the lowest power consumption, is a serious issue for detectors in modern HEP experiments and will be even more important for future experiments. Minimising the number of data lines in detection systems is crucial for readout electronics in proximity to sensor level as well as for intermediate transmission level between the detector and the data acquisition system. The LumiCal detector at future ILC will comprise of about 30 layers of sandwich type calorimetric Si–W planes [1].

* Presented at the Workshop on Timing Detectors, Kraków, Poland, November 29–December 1, 2010.

† Corresponding author: jmoron@agh.edu.pl

The works are ongoing on a possibility of using a low power fast serial cable links to collect the data within a single detector layer as well as for sending the data from each layer outside the detector. The main goal of this work is to design a first prototype of transceiver ASIC for fast serial data transmission in the LumiCal detector. Such ASIC could be used in readout electronics for multiplexing and sending out the data from a multichannel ADC as well as for data transmission out of each detector layer [2].

The transceiver architecture and the design of its most important blocks are briefly described in Section 2. A dedicated test setup built to verify the efficiency of data transmission and to test the functionality of transceivers blocks is described in Section 3. In Section 4 the results of preliminary measurements of the whole transceiver and its functional blocks are presented.

2. Transceiver design

The important design goals are: obtaining maximum serial transmission performance in the chosen AMS 0.35 μm technology, obtaining a wide and variable range of transmission frequency. The requirement of a variable transmission rate is set to make the transceiver a general purpose device but it is in conflict with the requirement of lowest possible power consumption. In addition, the first transceiver prototype should also provide a maximum testability. For these reasons the optimisation of power consumption is not a main concern in present design and is left for future developments.

The main blocks of transceiver are the transmitter (TX) and the receiver (RX) circuits, as shown in Fig. 1. Apart from the core transmis-

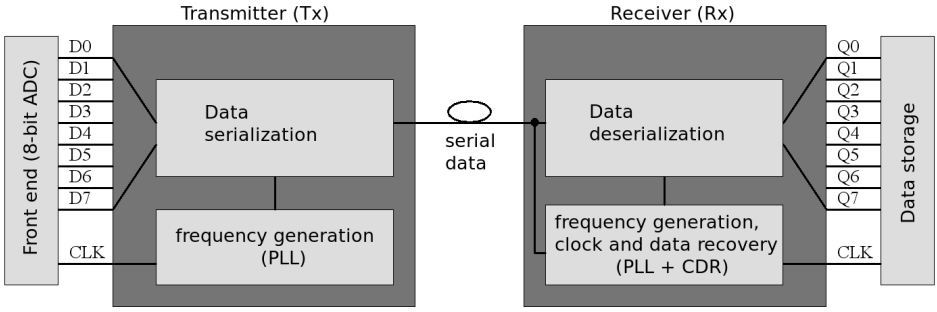

Fig. 1. Transceiver architecture.

sion/reception functionality the transmitter/receiver circuits provide the data serialisation/deserialisation. In this work a typical 8 bit data bus is implemented. A serial asynchronous differential transmission scheme is chosen in order to minimise the signal distortions between transmitter and receiver and to maximise the transmission rate. In addition to the transceiver circuit,

the prototype of designed ASIC contains also fast ($\sim$ 1 GHz) input/output LVDS (Low Voltage Differential Signalling) pads which are taken from earlier designs. In this work only the design of transmitter and receiver is described. The data coding and decoding, needed to provide enough slopes and DC line balance, is implemented in an external test setup.

The transmitter circuit contains a parallel synchronous to serial asynchronous data converter and a phase-locked loop (PLL) block for high frequency generation. The receiver circuit contains a clock and the data recovery circuit (CDR) which provides the clock synchronisation (based on data slopes) and a serial to parallel data conversion. When the transmitter is running, the data from an external circuit are read parallelly, synchronously with transmitter clock. After serialisation the data are sent to the receiver where, after clock recovery, they are converted from serial to parallel and sent (synchronously with receiver clock) to an external circuit. The internal PLLs are implemented in the transmitter/receiver to generate high frequency clocks used in data transmission/reception. A simple shift registers are used for data conversion in transmitter/receiver circuits.

Figure 2 shows a typical second order Phase Locked Loop (PLL). The "current starved" inverters are used in the design of Voltage Controlled Oscillator (VCO). To obtain a variable transmission range and a maximum testability the PLL is designed to work in four frequency modes: 120 MHz, 240 MHz, 480 MHz and 960 MHz, switched by changing the division factor in PLL feedback loop.

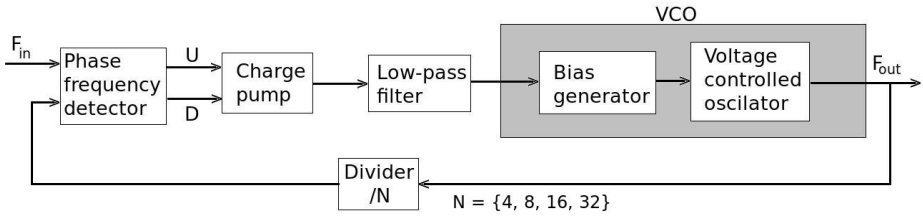

Fig. 2. Second order Phase Locked Loop architecture.

The clock synchronisation between the transmitter and receiver is provided by the CDR circuit [3] showed in Fig. 3. The "burst mode" architecture (Fig. 3, left) [4] with two extra gated voltage controlled oscillators (GVCO) [5] steered by the data signal levels are used for the clock recovery. A simple decision circuit with a D-type flip–flop (Fig. 3, right) removes the noise from input signal and regenerates the data waveform.

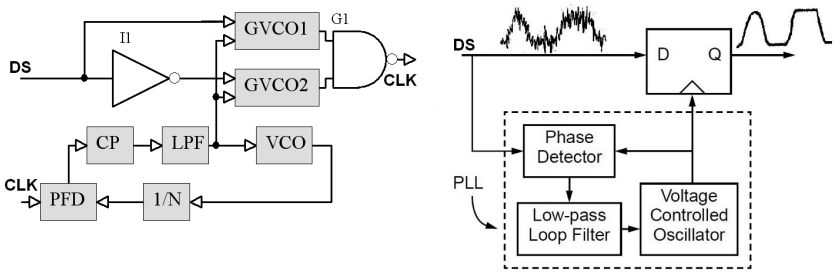

Fig. 3. Clock and Data Recovery — "burst mode" architecture (left); data recovery with decision circuit (right).

3. Test setup

A dedicated test setup was built to verify operation, in particular the serial data transmission efficiency, of the prototype transceiver ASIC. Its simplified diagram is shown in Fig. 4. The functional core of test setup is a fast data transmission loop: **Virtex5 FPGA → transceiver ASIC** and **transceiver ASIC → Virtex5 FPGA**, implemented to verify the transmission efficiency. The test data are transmitted between the Virtex 5 board [6] and the transceiver ASIC through 8 bit parallel data bus using fast LVDS buffers (transmission rate up to about 130 MB/s). The two internal fast RAM memory blocks of Virtex 5 board are used interchangeably for the transmission tests. In the first step the data are sent from the first RAM block to the transmitter while in the second step the data bus is switched to the second RAM block which stores the data from the receiver.

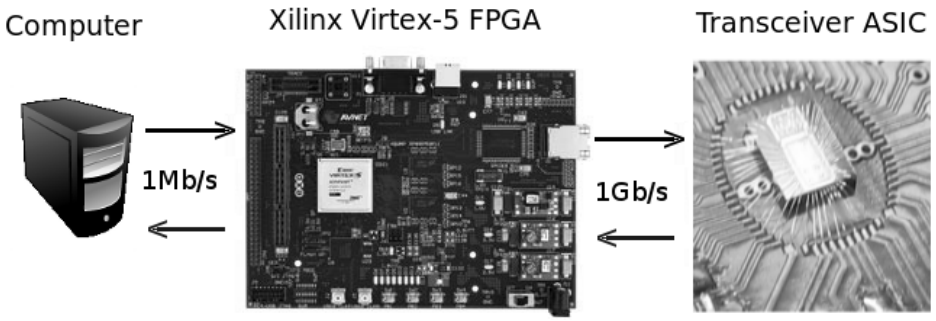

Fig. 4. Simplified test setup diagram.

The transmission between Virtex 5 board and PC computer runs on parallel 8 bit bus with much slower rate (about 1 Mb/s). An additional USB to parallel converter (FTDI FT245 device) is used for this aim on the PC side.

The C++ program is used to generate, code, decode and analyse the test data packages. A single package contains up to 32 kB (determined by the FPGA RAM size) of random data with 8b/10b coding. The packages are repeated 20 times for each measurement point what gives 640 kB per one measurement. The received data are compared with the generated package in order to find any possible data corruption. The transmission is considered 100% efficient if no error is found in the whole 640 kB data volume.

4. Measurements

A number of measurements are done to estimate quantitatively the transceiver performance as well as the performance of its main blocks. Here we present only the results of measurements performed in the most interesting highest frequency mode, *i.e.* in the 960 MHz mode. Similar measurements, confirming a good circuit functionality, were also performed for the slower modes.

The transceiver power consumption of about 45 mW is measured in the 960 MHz mode, at default 3.3 V bias. It gives ≈ 22.5 mW per transmitter and receiver. As already pointed the first ASIC prototype is not optimised for low power consumption. The preliminary simulations of next transceiver version show that the power consumption may be largely decreased, more or less by a factor of 4–5.

In the first measurements the operation of PLL circuit in the transmitter and receiver is verified. Figure 5 shows a two-dimensional working region of the transmitter PLL. It is seen that the PLL works correctly in frequency range from 420 MHz to 1090 MHz at default 3.3 V bias. The minimum working frequency is about 290 MHz at 2.0 V bias and the maximum frequency is about 1140 MHz at 3.5 V bias. The PLL works also in a wide power supply range from 2 V to 3.5 V. A very similar performance and working region is found for the receiver PLL.

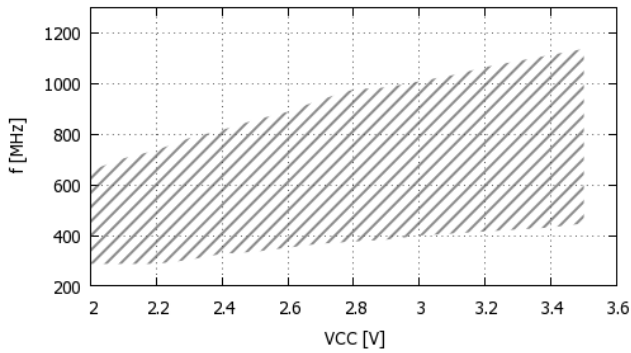

Fig. 5. Transmitter PLL working region.

Figure 6 (left) shows the receiver frequency spectrum measured using the Agilent 4395A spectrum analyser. When no data are transmitted, *i.e.* the transmitter is in idle state and the CDR circuit is not active, the measured receiver clock frequency is about $\approx$ 965 Mhz which gives 5 MHz (0.5%) offset from the fixed transmitter frequency of 960 MHz. When the data are transmitted (Fig. 6 right) the CDR circuit is active and the measured clock frequency of receiver is equal to the transmitter one. This confirms the correct operation of CDR circuit.

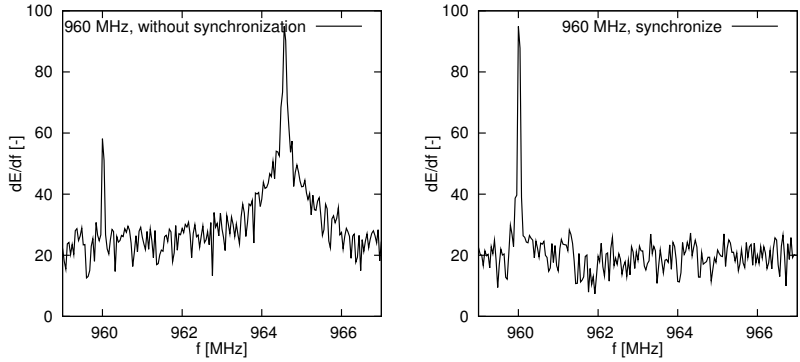

Fig. 6. CDR clock frequency distribution: no data transmitted, CDR inactive (left); data transmitted, CDR active (right).

In a final measurement an overall efficiency of data transmission between the transmitter and the receiver is verified. As described in the previous section the measurements are done transmitting the packets of 640 kB of data, coded in the PC before transmission and decoded again in the PC after reception. In Fig. 7 the dependence of data transmission efficiency in the 960 MHz mode *versus* the transmission frequency is shown, for default 3.3 V bias. It can be seen that a full 100% efficiency is obtained in the frequency range between 640 MHz and 976 MHz.

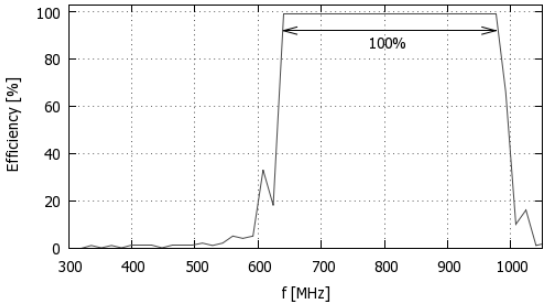

Fig. 7. The transceiver data transmission efficiency as a function of the transmission frequency.

5. Conclusions

A first prototype of the transceiver ASIC for fast serial data transmission, comprising of the transmitter and receiver, was designed and produced in the AMS 0.35 μm technology. The performed measurements showed that both the transmitter and the receiver are fully functional and work well in a wide frequency range. The quantitative measurement of complete transceiver efficiency was done verifying the data transmission between the transmitter and the receiver. It showed that the transceiver is fully efficient for transmission frequencies ranging from 640 MHz to 976 MHz. The results confirmed that a fast (about 1 GHz) serial data transmission may be obtained in the chosen technology and such a transmission is a valid option for the LumiCal detector at future ILC. In the next step the implementation of a transceiver optimised for a low power consumption is foreseen.

This work was supported by the Polish Ministry of Science and Higher Education under contract No. 1246/7.PR UE/2010/7.

REFERENCES

[1] W. Daniluk *et al.*, Redesign of LumiCal Mechanical Structure, Eudet-Memo-2010-06, `http://www.eudet.org/e26/e28`

[2] M. Idzik *et al.*, The Concept of LumiCal Readout Electronics, EUDET-Memo-2007-13, `http://www.eudet.org/e26/e28`

[3] R. Walker, Clock and Data Recovery for Serial Data Communications, ISSCC Tutorial, February 1997.

[4] M. Banu, A.E. Dunlop, *Electron. Lett.* **28**, 2127 (1992).

[5] P.-S. Han, W.-Y. Choi, *IEEE Trans. Circ. Sys. II* **54**, 38 (2007).

[6] Avnet, Xilinx Virtex-5 FXT Evaluation Kit — Product Brief, `www.em.avnet.com/ctf_shared/evk/df2df2usa/xlx_v5fxt_evl-pb052208F.pdf`