MEASURING TIME WITH A 5-PS PRECISION AT THE SYSTEM LEVEL WITH THE WAVECATCHER FAMILY OF SCA-BASED FAST DIGITIZERS*

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Test and characterization of the new generation of fast detectors are pushing the time precision required for associated electronics towards the picosecond level. The WaveCatcher board family has been developed for proposing a powerful alternative to ADC-based digitizers or oscilloscopes. It permits a 12-bit waveform digitization over up to 64 channels, with a 500-MHz bandwidth and a sampling rate up to 3.2 GS/s, together with a time precision better than 5 ps rms. Thanks to the powerful software developed for the boards, measurement is made easy since the PC is transformed into an oscilloscope. It also permits saving data files directly on disk. The WaveCatcher systems actually are great tools for characterization of detectors down to a few ps level. An increasing number of labs or companies are now using the WaveCatcher boards worldwide on their test benches or physics experiments.

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1. Introduction

Fast particle detectors are implied in an increasing number of applications. Fast signals can also be produced by captors mounted on particle accelerators. Associated electronics used for their characterization has to reach an ultimate performance level in order not to degrade their intrinsic resolution. As it will be shown in this paper, waveform digitizing with analog memories permits reaching this goal. Indeed, this solution offers a high level of integration but also a very high precision both for amplitude and time measurement, the latter reaching a few picoseconds level.

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2. Why analog memories?

The recent progresses in detector developments have raised the requirements for the associated readout electronics towards the picosecond level. This is, for instance, the case for the new generation of MCP-PMTs (Micro-Channel Plate PMTs), but also for the upcoming generations of diamonds and SiPMs. The usual solutions dedicated to precise charge and time measurements for test or characterization benches are mainly based on the use of high-end oscilloscopes. But their cost per channel is high and their number of channels very limited. Numerous test benches were also based on commercial modules, both Charge-to-Amplitude Converters and Constant Fraction Discriminators (CFD) associated with Time-to-Digital Converters (TDC). The time resolution obtained with some of these modules, like the ORTEC 9327CFD, TAC588, and 14-bit ADC114 electronics, is very good ($\sim$ 5 ps rms after time-walk correction), but they are expensive and house very few channels [1]. Some TDC boards offer a higher number of channels, using multi-channel TDC ASICs based on a coarse measurement performed by a digital counter associated with a fine measurement (interpolation) using Delay Line Loops, but their overall resolution is today limited to $\sim$ 25 ps rms. One of the reasons is the need for a discriminator to transform the incoming analog signal into digital in front of the TDC, which is a source of extra jitter. Recent works are reporting the integration of high-precision TDCs inside high-end FPGA with an impressive level of performance. But these solutions suffer from the need of a discriminator the same way the TDC ASICs do.

Digitization systems have actually followed the progress of commercial ADCs, but the latter exhibit large drawbacks like their huge output data rate and power consumption. They thus require the use of very high-end FPGAs to treat the data flux, thus introducing extra cost and complexity. Conversely, high speed analog memories now offer sampling rates far above 1 GS/s over 12 bits at low cost and with low power consumption [1]. Moreover, their companion FPGA can be low-end, thus also low-power and low-cost.

Recently, these progresses in the field of waveform digitizers permitted the development of alternative methods for amplitude, charge and time measurements. Based on digital treatment of detector signal, they permit a straightforward calculation of the charge and amplitude, and achieve a timing resolution far better than the sampling frequency thanks to signal interpolation.

3. Analog memories versus ADCs/TDCs

Analog memories are circular buffers, based on arrays of switched capacitors, which record the analog signal at (very) high rate and stop after trigger for readout and analog to digital conversion (see Fig. 1). They actually look like perfect candidates for high precision measurements at large scale. Indeed, like ADCs, they catch the signal waveform, from which any kind of information can eventually be extracted, like baseline, amplitude, charge, time, *etc.* The TDC functionality is built-in, as the position in the memory gives the time of the sample, which can even be absolute if said position is linked to a clock driving a time counter in parallel. Conversely to ADCs, only the useful part of the signal is digitized, which permits reducing the dataflow and the system power dissipation. On the other hand, their drawbacks are the limited recording depth linked to the physical memory size (usually few hundreds to a few k-samples per channel) and the readout dead-time if the number of read samples per event is large. Simultaneous write/read operation is feasible, which may further reduce dead-time if necessary.

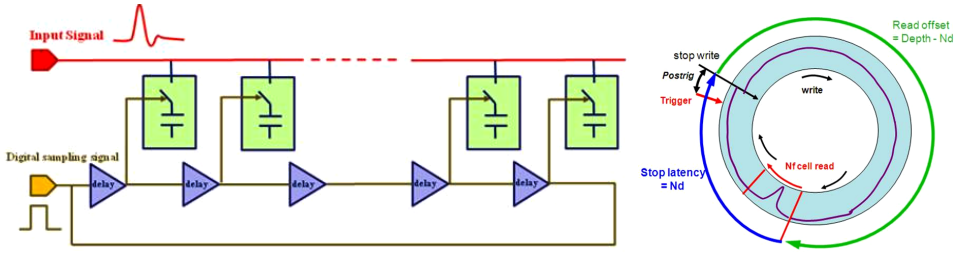

Fig. 1. Left: a write pulse is running along a servo-controlled delay line (DLL), emulating a high sampling frequency circular buffer. It drives the recording of signal into analog memory cells. Right: recording stops after trigger in order to perform readout and analog to digital conversion. Readout can target an area of interest, which can be only a subset of the whole channel.

4. Developments of ASICs and boards

4.1. The SAMLONG ASIC

The LAL/IRFU team has been developing analog memories since 1992, when the first prototype of the SCA for the Liquid Argon Calorimeter of ATLAS was submitted in AMS 1.2 μ CMOS technology. This project ended up with the HAMAC chip designed in 2003 in the radiation-hard DMILL 0.8 μ technology, of which 80,000 were produced and are on duty at the LHC since 2008. They participated in the discovery of the Higgs boson and

permitted a precise measurement of its energy. Many other circuits have been designed since 1999, split into three main families: ARS, MATACQ, and SAM which globally corresponds to 30,000 circuits currently used in many different experiments or systems.

SAM family ASICs are based on an analog matrix structure patented in 2001 (see Fig. 2) [2, 3]. This structure, in which the input signal is split into 16 individually buffered lines, permits having always only one single memory cell being written at a given time for a given line. The buffers ensure a high input impedance (which reduces crosstalk) and a high quality of the stored waveform, with the little drawback of increasing the power consumption. As the lines are short, their capacitance is small which permits offering a -3 dB wide signal bandwidth of 500 MHz with a reasonable power. Moreover, the clock-based matrix architecture ensures a perfect behavior of the chip for time measurements of events, independently of the physical location at which they are stored in the chip. Individual servo-controlled Delay Line Loops (DLLs) are located vertically in each column and ensure the virtual multiplication of the clock by a factor 16 for the equivalent high-frequency sampling (for instance 200 MHz to 3.2 GHz). Multiplexed readout is performed column by column, which makes it faster, and also permitted optimizing the Signal-to-Noise Ratio (SNR) of the readout amplifier.

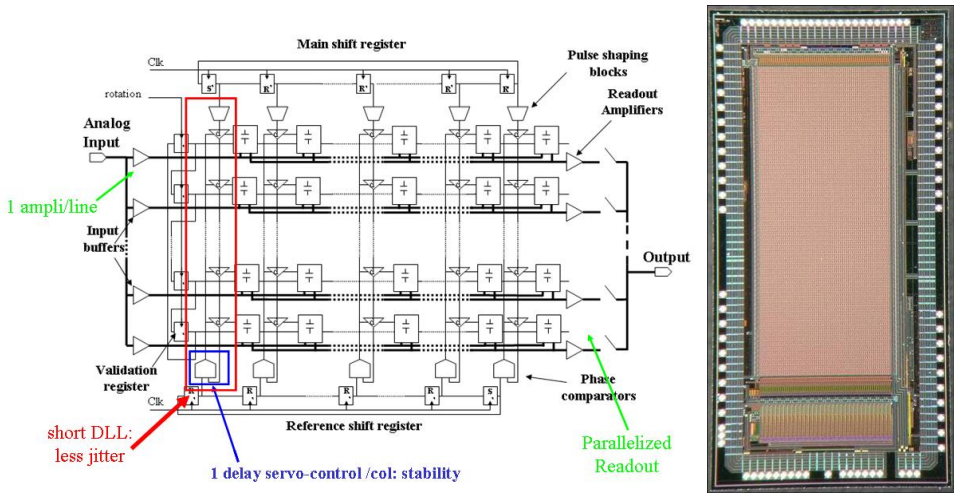

Fig. 2. Left: the matrix structure of the SAM ASIC family. Right: the SAMLONG chip, AMS 0.35 μm CMOS technology, 11 mm^2, 2 ch — 1024 cells/ch — 12 bits — 500 MHz — 3.2 GS/s. The chip is rotated 90° clockwise w.r.t. the matrix structure.

The SAMLONG chip used on the WaveCatcher boards is shown in Fig. 2. Its full-custom design houses 2 fully differential channels, each of 1024 cells (16 lines and 64 columns). It has been designed in the cheap pure CMOS 0.35 μm AMS technology and consumes $\sim$ 150 mW per channel. It houses 100,000 transistors over 11 mm^2. It is packaged in a small 100-pin 0.5 mm-pitch 14×14 mm^2 QFP package. Its high dynamic range ($\gg$ 12 bits) and high bandwidth (500 MHz) allow it to finely sample high speed signals like very short pulses, and make it very well suited for fast detector readout. Moreover, thanks to the servo-controlled matrix structure, the time parameters are very well mastered thus offering an impressive sampling time precision, equivalent to that of ultra-fast ADCs (see below). Many configuration registers are accessible via a SPI serial link. The chip is able to automatically swap the power between the input buffers and the readout amplifiers during the readout phase. On-chip DACs are located on each buffered line for line-offset compensation. When these DACs are tuned, data digitized at the chip output is good enough to be used directly for on-line calculation without any extra amplitude or pedestal correction.

4.2. The family of WaveCatcher boards

The family of WaveCatcher boards [4] has been designed to provide high performance measurements over a short time window. It houses between 2 and 64 channels based on the SAMLONG chip described hereabove. The boards are DC-coupled with unity gain, but could also be AC-coupled with a gain up to 15 (still offering 350 MHz of bandwidth). An individual DC offset can be added at input in order to get a full benefit of the 2.5 V dynamic range, and an individual trigger discriminator is available on each channel. This permitted the implementation of individual real time channel hit rate counters, independent of acquisition rate. All boards offer a lot of functionalities, like numerous coincidence trigger modes and an integrated pulse generator on each channel. They all house a USB 480-Mbits/s interface permitting an actual readout flow up to 30 Mbytes/s.

Fig. 3. Left: the 2-channel USB WaveCatcher module. Right: the 8-channel WaveCatcher module.

The 2-channel board [4] (see Fig. 3, left) is USB-powered. It integrates a block for calculating the pulse charge onboard, thus providing very fast histogramming for multiple photon-electron spectra. The board is packaged in a friendly plastic box. This permits using it comfortably together with a laptop, the latter being the source of power via USB.

All the other versions use a slightly different design, based on front-end blocks of 4 channels (see the example of the 16-channel board in Fig. 5). In addition to the aforementioned functionalities, they all include the capacity to perform real-time on-board feature extraction on waveform, like baseline, amplitude, charge, and time measurements. For the latter, time can be measured either by a digital Constant Fraction Discriminator (CFD), or by the crossing of a fixed threshold.

The first version embedding these features is the 8-channel module. Here, the front-end blocks are implemented as two daughter boards mounted on a motherboard. The module is packaged in an autonomous metallic box (see Fig. 3, right) and makes use of an external compact AC/DC switching adaptor power supply. UDP and optical links are implemented, but not yet active. This should however be the case very soon.

Next board version is the 16-channel board (see Fig. 4). It is the basis of all the system versions between 16 and 64 channels. It fits inside a VME-like 6U crate, but with a depth of 220 mm. Its rear VME P1 connector is used only for supplying the board when the latter is plugged into a genuine VME crate. Here, the front-end blocks are directly integrated on the board. USB and optical link are present on the front panel. In order to build the higher

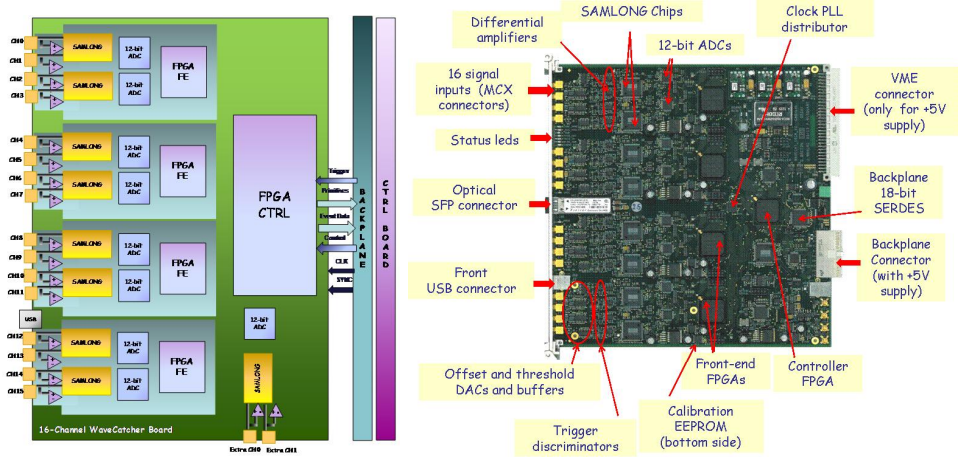

Fig. 4. Left: block diagram of the 16-channel board. The 4-channel front-end blocks are used in all the modules containing 8 channels or more. Right: the 16-channel WaveCatcher board.

scale versions of the system, a dedicated 2 mm-pitch backplane connector is available on the rear of the board. It permits controlling and reading it out via the custom backplane and thanks to the custom-designed LP Bus architecture described in Fig. 5, left.

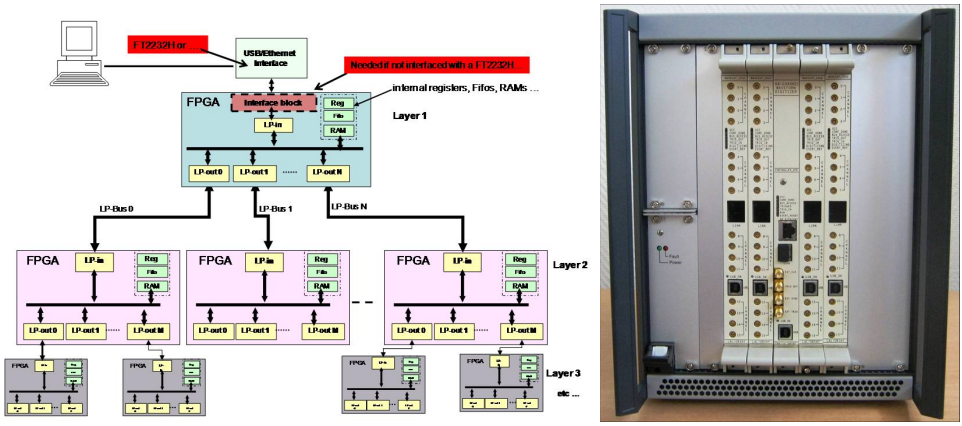

Fig. 5. Left: LP Bus, a multi-layer custom Control & Readout Architecture and Protocol. Right: the 64-channel WaveCatcher crate.

The last system version as of today is the 64-channel crate (see Fig. 5, right), which dimensions are as small as $11 \times 26 \times 30$ cm^3 (like a standard oscilloscope). It can house between one and four 16-channel boards, interconnected by a 5-slot custom backplane. It permits the control and readout of the boards, as well as the concentration of the trigger primitives toward the central controller board which computes the trigger, and houses all the bus and external signal interfaces.

In addition to the features already evoked, one can add the following ones: 2 extra memory channels for "digital" signals on 16-channel board (which can be used as additional analog inputs), external clock input for multi-board applications (8, 16 and 64-channel), possibility to upgrade the firmware via USB.

5. The acquisition software

In parallel to hardware and firmware developments, and in order to offer to the system users a Plug and Play interface, we developed a user-friendly and powerful data acquisition software running on Windows and transforming the PC into an oscilloscope (see Fig. 6). It is currently used for most applications of the WaveCatcher system.

The software described above embeds all features permitting an easy measurement and real-time histogramming of the information extracted from the signal, including the time difference between two pulses located on any channel.

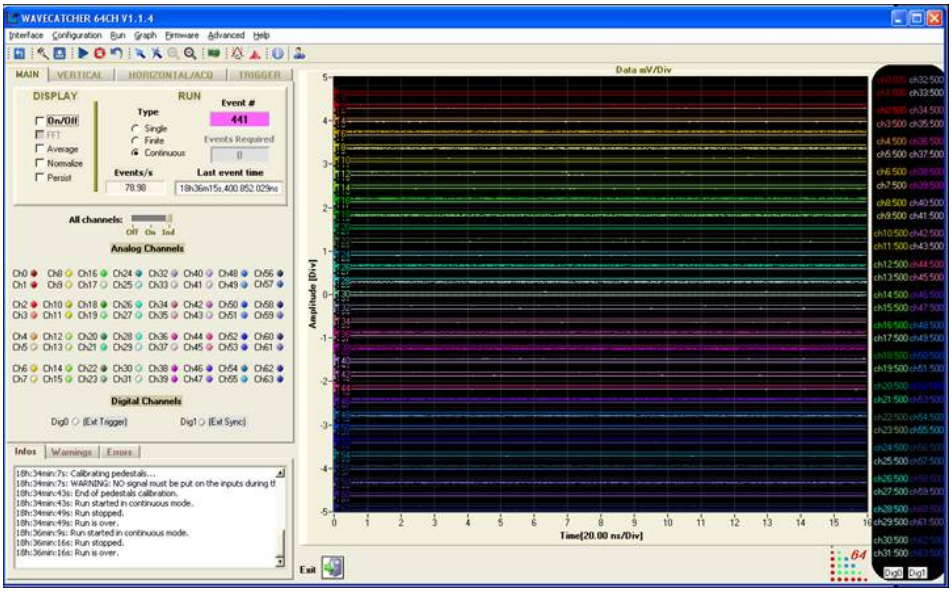

Fig. 6. Main panel of WaveCatcher acquisition software.

6. Measurement results

6.1. Quality of signal

The main goal of the WaveCatcher system is to offer a high performance waveform digitization, both in terms of signal measurement quality as in term of data readout. Special care has been taken in the design in order to optimize the SNR and reduce any kind of crosstalk despite the vicinity between wide range DC-coupled analog signals and fast digital activity. Analog inputs are unipolar (terminated on 50 Ω), but immediately transformed into differential at the board input. Signals then remain differential until they reach the ADCs. Noise level is of 0.7 mV rms, with a dynamic range of 2.5 V, centered around zero by default. The non-linearity remains within ±1% over the whole dynamic range. The custom-designed LP Bus architecture permits feeding the maximum bandwidth into USB, and usual limitation is rather linked to the software or to its capacity to save waveform data on disk.

One of the important characteristics of the WaveCatcher is that very few calibration steps are necessary in order to obtain the best performance of the system:

— Offsets of trigger discriminators thresholds;

— Line offsets (internal to SAMLONG);

— Optionally: residual of individual pedestals;

— Time Integral Non-Linearity (Time INL: see below).

All these calibrations are performed by the WaveCatcher software and results are stored in the on-board EEPROM.

6.2. Time measurements

Another important goal of the WaveCatcher system was to give the possibility to perform high resolution time measurement over all input signals. Like interleaved ADCs in the high-end oscilloscopes, analog memories need to be calibrated in order to get rid of the non-perfectly equidistant time between samples. The deviation of the real sampling time to the ideal one is mainly related to the position of the sampling cell in the chip. The characteristic giving this deviation as a function of the cell index is called time INL and will be used to correct the timing of the raw data.

In order to perform time INL calibration, we use a method we introduced in 2009 [4], and apply since with all our analog memories. It is based on a single run with a free running asynchronous sinewave whose frequency is close to that of SAMLONG's main clock. We take benefit that, conversely to TDCs, the information contained in a sample is not just binary. We only use the zero-crossing segments of the signal, with the main assumption that the sinewave is nearly linear in its zero crossing region: this is much more precise than the usual statistical distribution used for TDCs.

In order to check the calibration, we use, for instance, an AFG 3252 arbitrary generator from Tektronix. In the example below, we sent 2 pulses distant from $\sim$ 10 ns, with a 2.5 ns risetime, a width of $\sim$ 4 ns and an amplitude of 1.2 V (see Fig. 7).

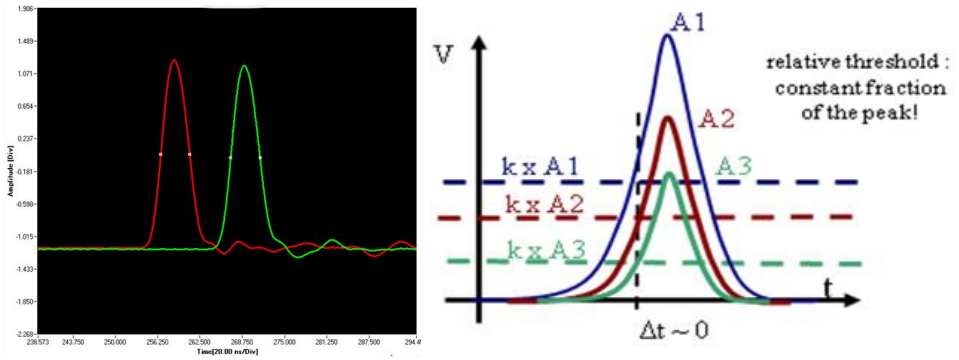

Fig. 7. Left: the 2 pulses used for time measurement as recorded by the WaveCatcher board. Right: the principle of the digital CFD algorithm.

We then measure the time difference between the two pulses in digital CFD mode both with the software and with the on-board embedded feature extraction. One can notice in Fig. 8 the quality of the measurement: below 5 ps rms for Δt, which corresponds to $5/\sqrt{2} = 3.5$ ps rms resolution per single pulse. It has to be noted that the on-board feature extraction performed in the FPGA (then INL-corrected by software) gives almost the same result as the full software calculation. This is due to the quality of the raw data produced by the SAMLONG chip, and permits envisaging the option of using the system without sending the waveforms, which would drastically reduce the dataflow and thus increase the acquisition rate.

Another important feature is that the SAMLONG chip is based on multiple DLLs locked on the same clock, which implies that there is almost no effect of the distance between the pulses on the jitter of the Δt measurement, even up to 10 s of μs.

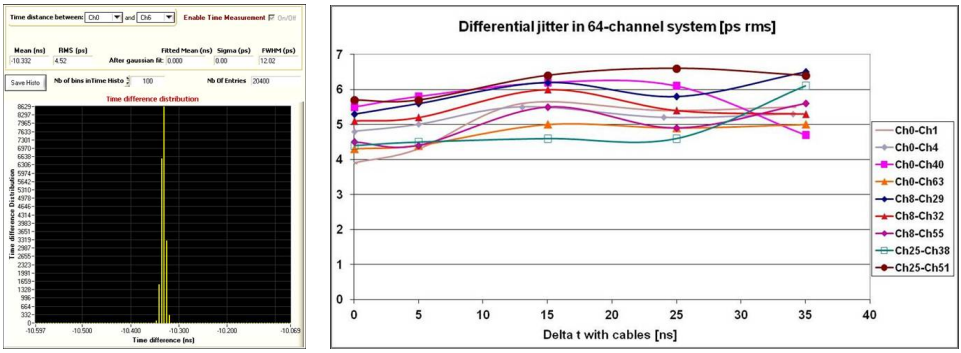

Fig. 8. Left: histogram of Δt between the two pulses of Fig. 7 = 4.52 ps rms. Right: jitter on Δt measurement in the 64-channel system, measured with cables.

Figure 8, right shows a measurement with a 64-channel system of the differential jitter for pulse distances ranging between 0 and 35 ns. This delay has been introduced via cables in order to get rid of any parasitic source of jitter. One can notice that:

1. The differential jitter between channels is as low as 4 to 7 ps rms, almost flat and independent on channel location.

2. Even between different boards, the jitter remains of the same order than between closely neighboring channels.

6.3. Effects of temperature

Except for the time precision, there is no major dependence of system performances to temperature if the latter remains below 50°C. Noise levels remain unchanged and pedestals may drift by a few hundred μV. On the other hand, time measurement undergoes a small drift of 0.5 ps/°C.

7. Summary of performances

		Unit
SAMLONG ASIC technology	AMS CMOS 0.35 μm	
System number of channels	2, 8, 16, 32, 48, 64	
Power consumption	2.5 (2-ch), 15 (8-ch), 23 (16-ch), 100 (64-ch)	W
Sampling depth	1024/channel	Cells
Sampling speed	0.4 to 3.2	GS/s
Bandwidth	500	MHz
Range (unipolar)	$\pm$1.25 (with full range individual channel offset)	V
ADC resolution	12	bits
Noise	0.75	mV rms
Dynamic range	11.5	bits rms
Readout time	11 to 66 (depends on number of cells read)	μs
Time precision before correction	< 20	ps rms
Time precision after time INL correction	< 5	ps rms

8. Conclusion and future developments

In most cases, the WaveCatcher digitizers offer a powerful and low cost replacement for oscilloscopes and commercial ADC-based digitizer boards, especially for fast detector characterization. They are very well suited for

studying new-generation fast detectors down to a few ps rms resolution. Their sole limitations are linked to the sampling depth and the intrinsic deadtime which may limit the trigger rate.

Commercial products based on SAMLONG, equivalent to the 8- and 16-channel versions are available in the CAEN company catalog under the X743 digitizer family code.

The long years of R&D described in this paper have led to the filing in 2009 of a new patent for the so-called "Waveform TDC". The corresponding ASIC has been designed and mounted in an acquisition module in the frame of the SAMPIC project which was presented in the same workshop [5].

Concerning the future developments, a new version of SAMLONG should be submitted soon. The latter will optimize certain internal parameters, permit a faster readout and offer a reduced noise level. Firmware and software upgrades will also be pursued, mainly on demand from the numerous system users.

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