

WHITE RABBIT TIMING RECEIVER FOR MICRO TCA-BASED DATA ACQUISITION SYSTEMS FOR APPLICATIONS IN HIGH ENERGY PHYSICS*

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The Micro TCA (MTCA) platform gains popularity in modular measurement and control systems. Version 4 of the standard is well-suited for high-energy physics and is intensively developed by leading scientific institutions including CERN and DESY. While being primarily developed for low-level RF applications, it is currently being implemented in numerous data acquisition systems for detectors. This paper presents development of the distributed clock and event synchronization in MTCA.4 for large data processing systems based on White Rabbit protocol.

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1. Introduction

Micro TCA [1] is industrial standard with strong scientific community support. Together with version 4 and introduction of RTM modules and dedicated trigger/interlock bus, it gained strong interest in accelerator science. While AMC modules are well-suited for FPGA technology, high speed connectivity (40 G), management and digital processing, RTM is best suited for analogue front-end including RF and low-level signalling. Recently introduced RF backplane [2] together with low jitter clock module and low noise supplies offers excellent environment for mixed signal systems. While MTCA.4 operation was proven in low-level RF applications, it has some limiting factors in the case of multi-channel detector systems. An example of such system is readout and processing of signals from Gas Electron Multipliers [3] and other multi-channel detectors. In such systems, additional features are required:

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- Timing receiver which synchronizes operation of all the experiment sub-systems with sub-ns accuracy and provides crate-wide timing reference;
- Distribution of low jitter clock references with different frequencies locked to same reference, common for whole detection system and also accelerator RF;
- Trigger and interlock distribution and time stamping generated by timing receiver or DTC block.

It is possible to build such setup using dedicated AMC board with timing receiver [4], such approach has several limitations:

- Degradation of clock signal jitter which need to be passed by MCH-CLK module and distributed to all AMC boards;
- Occupation of precious AMC slot of MTCA crate, critical in small form factors;
- Lack of MLVDS and CLKA/CLKB synchronization due to different signal paths. MLVDS are routed directly, while CLKA/CLKB go via MCH-CLK module.

There are also dedicated timing receivers which occupy redundant MCH [5] but still have no access to the M-LVDS lines and are able only to generate timing reference. Due to the facts stated above, proposed is novel solution which extends functionality of existing N.A.T. MCH family [6].

2. White Rabbit MTCA Timing Module

The WR-MCH clock module extends functionality of existing N.A.T. MCH by redundant White Rabbit receiver capability [7]. It is tightly coupled with existing Tongue 1 management board and Tongue 3 PCIe Hub module and replaces existing Tongue 2 clock distribution board.

The WR-MCH solution is dedicated to low-level RF, signal detection, processing and real time control applications. The main feature is ability to generate custom clock signals locked to the main WR clock with any frequency and phase locked to the source installed within WR network [8]. The block schematic of WR-MCH is presented in Fig. 1. The module consists of following blocks:

- Dual, redundant White Rabbit (WR)/PTP timing receiver which synchronizes operation with sub-ns accuracy and provides crate-wide timing reference over the M-LVDS bus. It is also possible to implement other custom time synchronization protocols like SyncE or TTC [9];

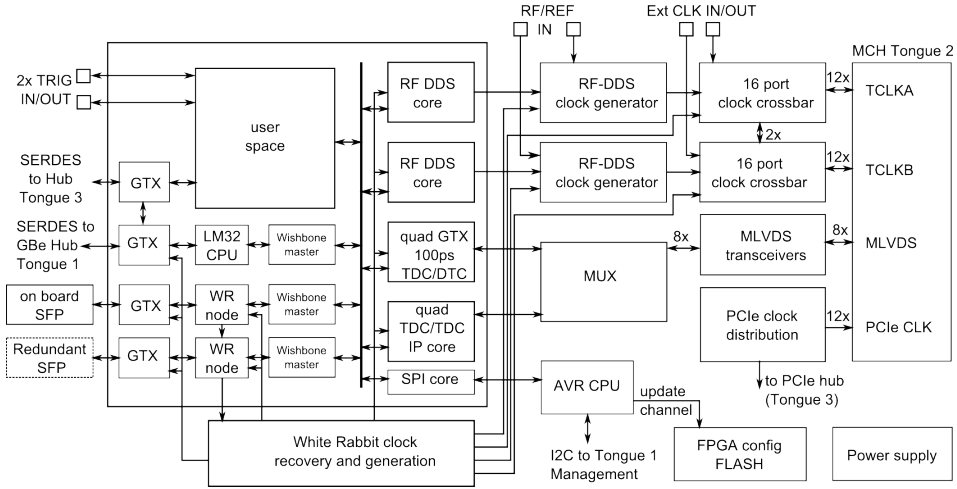


Fig. 1. WR-MCH schematic block.

- Distribution network of low jitter clock references with up to two different frequencies locked to same WR 125 MHz reference, common for whole WR domain. Dual, ultra-low jitter bi-directional MTCA-compliant clock mux for both CLKA and CLKB clock trees is used;
- Dual channel DDS-RF generator. It provides ability to generate any frequency which is phase-locked to the source installed in any place of WR network;
- Trigger and interlock distribution circuit;
- 8 channel time stamping circuit providing 1 ns resolution;
- GPS UART, PPS and clock inputs (available on double width panel only).

Figure 2 presents drawing of the complete WR-MCH module. The WR — clock module fits into existing N.A.T. MCH and is compatible with single and dual width MCHs, including NAT-PHYS. Single width offers single SFP connector, while double width offers two SFP cages and several additional clock and RF signal connectors.

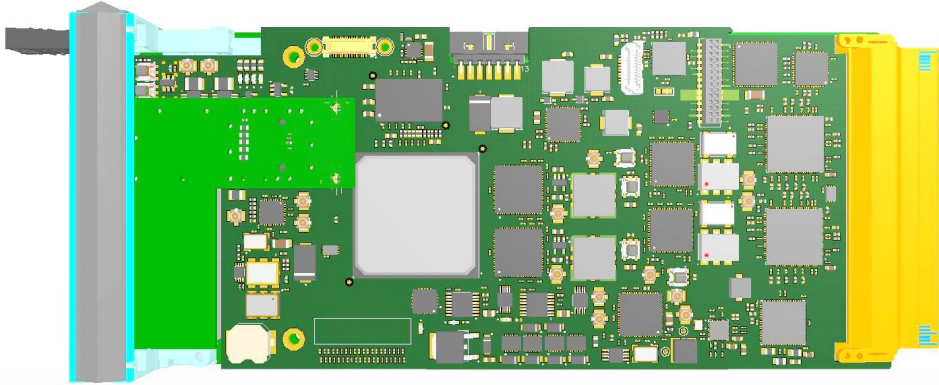


Fig. 2. View of the clock module installed on the top of N.A.T. MCH (PCIe hub not shown).

3. Summary

The WR-MCH timing module will find applications in several high-energy physics experiments and hot plasma diagnostics in Tokamaks [10]. It solves several issues related with timing, clock distribution and together with N.A.T. standard MCH provides complete and scalable platform for both simple (based solely on WR Ethernet) and complex (PCIe-based) measurement and control systems. It can be additionally equipped with RF-backplane which is now fully supported by the N.A.T. MCH. Such complete solution is an ideal platform for many yet unknown applications of the MTCA platform.

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