OVERVIEW OF MICROELECTRONIC CIRCUITS DESIGNED AT AGH UNIVERSITY FOR THE CBM EXPERIMENT*

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This paper briefly summarizes the development and research work conducted at the AGH University contributing to the Compressed Baryonic Matter experiment at the Facility of Antiproton and Ion Research, Darmstadt, Germany since 2009. The need for microelectronic solutions enabling acquisition of data from the detector layers in the experiment led to the development of five small and two full-size prototype integrated circuits supporting the development of final multichannel integrated circuit SMX2.2 which will be used to build the Silicon Tracking System (STS) and Muon Chamber (MuCh) detectors. The aim of the read-out circuits is to aggregate the charge generated in the detectors, amplify and filter this signal and digitize the amount of generated charge and assign a timestamp to each event. The self-triggered, data-driven approach of hit data generation is implemented in this experiment. Overview of pre-studies of the Time-over-Threshold charge processing technique, shaper-based two path pulse processing, leakage current analysis and cancellation techniques are briefly summarized in this paper and referenced to the full papers on each of the presented topics. All the presented integrated circuits were fabricated using UMC 180 nm CMOS process.

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1. Introduction

The Compressed Baryonic Matter experiment is one of the scientific pillars of the Facility for Antiproton and Ion Research, being currently constructed in Darmstadt, Germany. It sets new, ambitious targets for experimental physics. Nucleus–nucleus, proton–nucleus and proton–proton collision products need to be identified and measured with unprecedented precision and statistics compared to the existing experiments [1]. The Department of Measurement and Electronics, AGH University, since ten years has

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been involved in development of integrated circuits for sensors read-out in the Silicon Tracking System (STS) and Muon Chamber (MuCh), parts of the CBM experiment.

The STS measures the charged particles' tracks and momenta using eight detector stations located between 30 cm and 100 cm from the target, inside the 1T magnetic field. Detector modules will be assembled using the 12 cm wide double-sided, stereo-angle silicon detectors (2 cm up to 12 cm long) connected to the read-out electronics via the custom-made, 4-layer aluminum, ultra-light micro-cables, which length can range up to 47 cm. This sets the channel pitch for 58 μm. Particles crossing the detectors' active area will generate electrical change, which will be amplified and measured (both arrival time and amplitude) in the integrated circuits (ICs).

Contrary to the other experiments, the CBM will not use trigger signal for selecting the interesting events for digitization and transmission. Detection of rare probes imposes using self-trigger (or free-streaming) architecture of the ICs and on-line track reconstruction. This approach requires particle arrival time (resolution better than 5 ns) and charge measurements (with resolution at least 0.5 fC) by faster analog-to-digital conversion (average rate of 250 kHit/s/channel) in each channel and fast data transmission. To minimize noise-related hits, it is crucial to provide low-noise measurement circuits (approx. 1000 e^- r.m.s.) at the power budget of 10 mW/channel. Expected beam intensity fluctuations require that ICs provide throttling and fast recovery features preventing from data link overflow leading to the loss of important data. The ICs need to provide immunity to radiation doses aggregated over 10 years of operation.

2. Preliminary studies

The key point was to choose the analog front-end (AFE) architecture for effective time and charge digitization method. One of the promising techniques was Time-over-Threshold (ToT) based processing. It uses the Wilkinson-type analog-to-digital conversion concept and measures the pulse width as it relates to the amplitude. The typical A/D converters (*e.g.* SAR — successive approximation register, or FLASH) implemented in each or one for several channels of the AFE, compared to ToT, ramp up the circuit complexity, area, and power consumption. However, obtaining a linear transfer characteristic of ToT processing, while keeping the low-noise performance is an actual research topic. Typical ToT circuits discharge the charge-sensitive amplifier's (CSA) feedback capacitor by the constant current source. The length of the resulting triangular output shape is then proportional to the input charge, so the transfer characteristic is linear, which was proven in pixel applications, where sensor capacitance is low (< 200 fF). Existing ToT solu-

tions for microstrip sensors (capacitance > 1 pF) resulted in nonlinear transfer characteristics due to the use of shaping amplifiers. AGH has fabricated two prototype, miniasic circuits (1.5 mm × 1.5 mm die size) TOT01[2] and TOT02 aiming at achieving the goal for the STS detector system. Finally, a DSToTIC [3] circuit was proposed (Fig. 1). Using two amplifying stages and splitting the functionalities, it was possible to isolate the competing requirements what enabled better optimization of these stages (*e.g.* providing large enough effective input capacitance and collecting the entire charge generated in the sensor, correct operation of the constant current discharge circuit even for low input charges). This resulted in a linear (INL = 0.83%) ToT transfer characteristics achieved for tens of pF of sensor capacitance. Essential components of the proposed solution included the digitally assisted reset circuits, which made the circuit faster and overload-proof. The gain is tunable (100–600 ns/fC). The voltage gain spread is low: 227 ± 5.54 mV/fC. The power consumption of this circuit is 2.5 mW/channel. The circuit can process 2 fC input pulses with maximum 2.5 MHz frequency. Achieved noise level is ENC = 273 + 51.8 × Cdet e^- r.m.s. Resulting performance, ability to measure arrival time and amount of charge (with linear transfer characteristics) demonstrated competitive advantages of the proposed solution in some application niches.

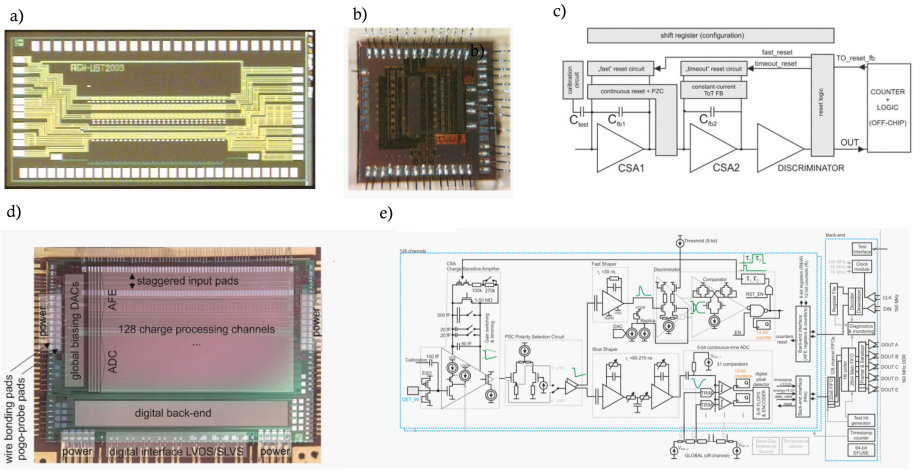

Fig. 1. (a) TOT01, (b) DSToTIC micrographs, (c) schematic of the DSToTIC, (d) SMX2 micrograph, (e) schematic of the SMX2 IC.

3. SMX or STS-XYTER series ASICs

The series of full-size (10 mm × 6.75 mm die size, 128 channels) read-out circuits for CBM STS was named STS-XYTER (Silicon Tracking System

X & Y Time and Energy Readout), or SMX. The first prototype, STS-XYTER1 [4] was designed at AGH in parallel with the ToT solutions to evaluate different AFE approach and building early prototypes of the detector module at FAIR. The charge-sensitive amplifier is driving two parallel signal paths built of CR-RC^n-type shaping amplifiers whose transfer functions were optimized for accurate time measurement (fast shaper, leading-edge comparator, and timestamp latch) or low noise amplitude measurement (slow shaper, continuous-time FLASH ADC [5]).

Detector system noise level depends mostly on the sensor capacitance, read-out ICs performance (determined by architecture, filter's characteristics, type, dimensions and biasing of the input transistor, layout-related aspects, series resistances, *etc.*) but also other parameters (*e.g.* parasitic components of the detector and interconnect). The unique set of these aspects in the STS detector makes it difficult to achieve the required parameters. It was necessary to build simulation models accurately representing the structure of this complex system [6] and analysis of the supply-noise impact on the performance, *etc.* [7].

Specification update resulted in development of major revision of the IC, named SMX2 [8] (Fig. 1). The list of new features and improvements includes: further noise optimization of the front-end, support of gaseous sensors for MuCh detector, upgraded baseline recovery circuit (CSA reset), redesigned digital back-end [9] as a result on new DAQ system in the detector, co-design of the AFE and power delivery network, STS power system and detector-cable, improved time measurement circuit, *etc.* Testability feature included on-chip diagnostic ADC [10], and support of the pogo-pin test station for validation of the detector-IC connectivity without wire-bonding [11]. STS will contain more than 1.7 million read-out channels created by more than 14 000 SMX2 ICs which are configured and read out by the custom data acquisition (DAQ) system [12]. The CERN-developed, radiation-hard data concentrators and optical transceivers, named GBTx connect the SMX2 ICs via the optical links (more than 4000 in the STS) to the higher-level systems, partially developed at the Warsaw University of Technology (WUT). The SMX2 chips communicate AC-coupled differential SLVS links using dedicated communication protocol [13] developed by joint effort of AGH, FAIR and WUT. It enables fast and effective hit data transfer and robust configuration and control messages as well as synchronization of time measurement.

4. Further developments and summary

Evaluation of the ICs revealed several weaknesses. One of them was the nA-rage leakage current resulting from MOS-based electrostatic discharge

(ESD) protecting circuits having strong impact on the CSA reset circuit performance [14]. This has lead to the development of two experimental AFEs to address this and several other problems like noise performance change due

TABLE I

Summary of presented ASICs.

IC name Year	Processing type	Equiv. Noise Charge (Q measurement)	Comments
TOT01 (2010), TOT02 (2011)	Time-over-Threshold, single stage	slope: $22.4\,e^-/pF$	first prototypes approaching problem with large sensor capacitance, − problems with charge collection at large capacitances, − processing time dependent on the input charge.
DSToTIC (2012)	Time-over-Treshold, dual stage	slope: $51.8\,e^-/pF$	+ enhanced charge collection at large capacitance, − processing time dependent on the input charge, − noise slope.
STS-XYTER (2014)	comparator, FLASH ADC, 2-path	—	first full-size prototype using CBMnet communication, − noise performance to be improved.
STS-XYTER2 (2016)	comparator, FLASH ADC, 2-path	slope: $27\,e^-/pF$	+ adaptation to the new DAQ system (new protocol and interface), − functional improvements needed (*e.g.* 10× more precise threshold setting in the ADC), − ESD protection leakage prevents use of fast reset.
SMX2.1 (2018)	comparator, FLASH ADC, 2-path	slope: $22\,e^-/pF$	no ESD protection on input pads (separate ESD chip), + multiple noise performance improvements, + the chip meets the CBM specifications (*e.g.* noise), − ESD protection needs to be on-chip.
ESD-CHIP (2018)	N/A; experimental ESD protection	N/A	− MOS-based protection is fast, but leakage current is high (above few nA), + diode-based protection result in very low leakage (below 100 pA).
SMX2.2 (2020)	comparator, FLASH ADC, 2-path	during fabrication	+ diode-based ESD input protection on-chip, + doubled protection on LVDS I/O, + minor digital fixes, + to be used in experiment assembly.

to the variable conditions and power supply interference coupling. Two prototype ASICs 1.5 mm × 1.5 mm each were developed at AGH and fabricated using 180 nm CMOS process. These front-ends comprise standard single-ended channels based on the SMX architecture and new pseudo-differential channels for the supply noise handling. For the adjustment of the charge processing chain to provide optimum noise performance, shaping amplifiers architecture and peaking time was made configurable. The leakage current compensation technique proposed and implemented in both chips is a novel combination with pulsed reset and double-polarity Krummenacher based feedback circuit [15].

SMX2.1 together with a separate, experimental ESD-TEST IC were fabricated to evaluate the performance of almost 30 different diode-based and MOS-based ESD protection circuit architectures in terms of leakage and noise added. As a result, a bulk-diode devices were selected for inclusion in the final revision of the ICs.

The pilot run of the final revision of the SMX2.2 chip is currently being taped out. It includes set of modifications tightly adapting it to the STS and MUCH conditions. After testing and full-volume production, it will be used to assemble the STS and MuCh detectors at FAIR, helping in new physics research. All the presented Integrated Circuits were fabricated using UMC 180 nm CMOS process using Imec services (mini@sic and engineering run) and the summary is presented in Table I.

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